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All Optical Universal logic Gates Design and Simulation using SOA

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Abstract

All optical logic gates are the building blocks of optical signal processing devices. In this paper, we propose all optical universal logic gates NAND and NOR gates based on four-wave mixing (FWM) in SOA. Logic levels at the output will be differentiated by the output power. Simulation has been performed at 40 Gb/s and extinction ratio achieved for NOR gate is 7.5dB and for NAND gate is 8.75dB.

I. INTRODUCTION

For many years, optics scientists have been looking for all-optical signal processing materials that enable one light beam to be controlled by another. However, most optical materials are linear and allow light beams to pass through without alteration. The key to achieving all-optical processing functions is to use a nonlinear optical material where different light beams can interact. Of the many nonlinear materials investigated, one device has emerged as a practical solution for all-optical signal processing the semiconductor optical amplifier (SOA). All-optical signal processing is particularly of interest in telecommunications applications, where the benefits of the optical approach in terms power and cost are becoming important. Today's telecom networks are based entirely on electronic data handling, but now the core network data speeds are at 40 Gb/s (40 billion bits per second) [1], and, instead of the cheap CMOS silicon devices that formerly handled these signals, specialist electronic materials and sophisticated radio- frequency techniques are required. The electrical signals are also more difficult to route and transmit at these speeds, which require more power and cost more.

In order to meet the ever-increasing demand of data communication for future optical networks, high-speed digital processing is required. Photonics signal elaboration at the optical layer is attractive to perform various computational functionalities, such as packet buffering, bit-length conversions, header processing, switching, retiming and reshaping, and overcoming all the speed electronics limitations. In recent years, a lot of effort has been spent in these fields and all-optical digital processing seems to be one of the most promising technologies to bring increased capacity, flexibility, and scalability to the next generation systems in the optical domain.

Due to their great potential in optical computation, several all optical Digital devices have been proposed as building elements for more complex subsystems, including optical threshold functions, logic gates[1], buffers , flip-flops[2], shift registers , and binary counters, exploiting nonlinear effects of semiconductor optical amplifiers(SOAs).

Integrated Mach-Zahnder interferometers (MZIs) [3] incorporating semiconductor optical amplifiers SOAs in the interferometer arms have recently been developed as very high-speed all-optical switching devices. Switches of course, are the vital component of a fibre optic communication network. Since electronic switching is a well develop technology, it would seem natural to use these switches in fiber optic networks. However the price for using this mature technology is optical to electrical (O/E) conversion with all the associated draw backs of this method. O/E and E/O conversion can be done only for a specific bit rate and data format. In addition, the high power consumption and cost associated with the amount of electronic equipment required diminish the attractiveness of this switching. Here optical gate design has been given, which can be used in optical switching as well as in optical memory.

II. DESIGN OF UNIVERSAL GATES

As we know that NAND and NOR are the universal gates and with the help of these gates we can

design any combinational circuit and these gate are also very helpful in designing sequential circuits also. In this paper we have presented the design of optical circuits generating logic of NAND and NOR gate by exploring Four Wave Mixing. Block diagram of NAND and NOR gate is shown in fig. 1.

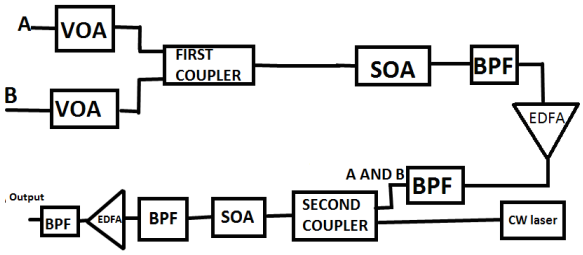

Fig 1(a) Block Diagram of optical NAND gate

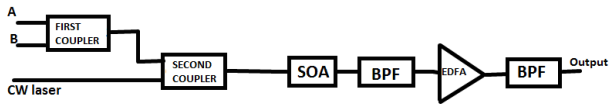

Fig 1(b) Block Diagram of optical NOR

A. Design & Simulation of optical NAND gate

A CW laser and the output of AND gate [2] is used to design the optical NAND gate as shown in fig1 (a). Two data pump generators (transmitter A and B) which carry digital data have been used to get the desired input signal. The circuit consists of optical AND gate [2]_and a probe pump (CW laser) combined at the second coupler as shown in fig 1(a). the combined output of AND gate and CW laser is given as input to the SOA, the output of AND gate is high '1' only when both the data pumps are at logic '1' otherwise it is low '0', So the FWM will generate at SOA only when both the data pumps are high'1'. If any of the data pump is at logic '0', output of AND gate will be low and the output power of SOA will be corresponding to CW laser only, which will show a logic high level because the power of CW laser is filtered and amplified to get the NAND gate output. If both the data pumps are high then the generated FWM signal at SOA will spread the power of CW laser and a lower power level is obtained at the center frequency of CW laser.

Working principle and circuit operation is described by frequency domain analysis and the logic is generated by power calculation at the output corresponding to different combination of logical input. Frequencies of data pumps and probe pumps are taken as below.

f_A = 193THz, f_B = 193.1THz, $f_{CW\ laser}$ = 192.9

Since FWM will generate only when more then one signal of different frequency is given at input of SOA [4]. At the input of SOA, AND gate output and CW laser is coupled. When any/both the data pumps are at logic '0', no FWM will be generated because output of AND gate will be '0' and the output will be corresponding to the peak of CW laser, as shown in fig 2.

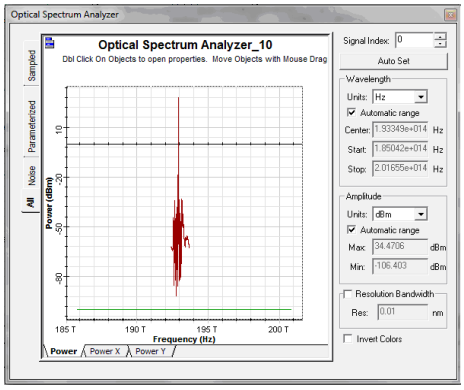

Fig 2: Sectrum analyzer at the output of second SOA when both inputs are low

Output of AND gate is high only when both the inputs are high so the output of AND gate and CW laser will together generate the FWM signal as shown in fig 3.

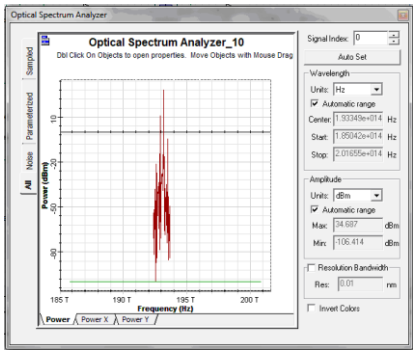

Fig 3: Spectrum analyzer at the output of second SOA when both inputs are high

Output of SOA is filtered with the BPF of center frequency of CW laser. This filtered output is amplified by linear amplifier i.e EDFA and is again filtered with the BPF to remove the unwanted signal. So a lower value of output power will be obtained when FWM will be generated and output will be considered as logic "0". For output power calculation time domain visualizer and power meter has been used for different input sequences as shown in fig 4-7.

1. A=0 and B=0

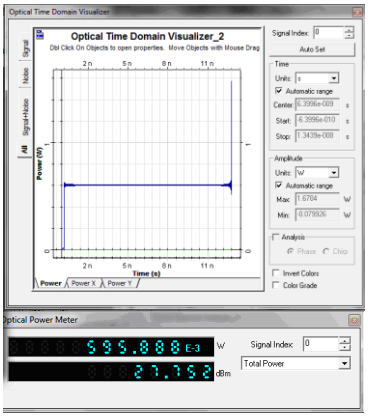

Fig 4: Time domain visualizer and optical power meter output at A=0, B=0

2. A= 0 and B=1

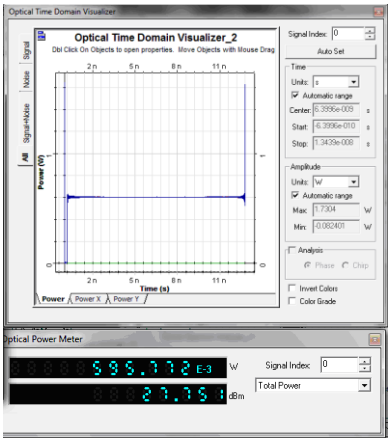

Fig 5: Time domain visualizer and optical power meter output at A=0, B=1

3. A=1 and B=0

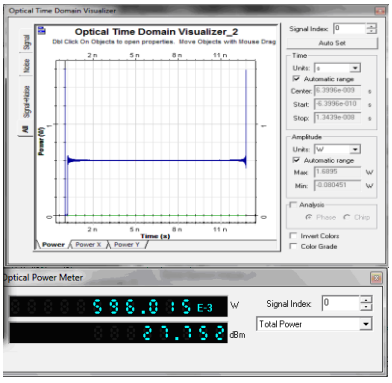

Fig 6: Time domain visualizer and optical power meter output at A=1, B=0

4. A=1 and B=1

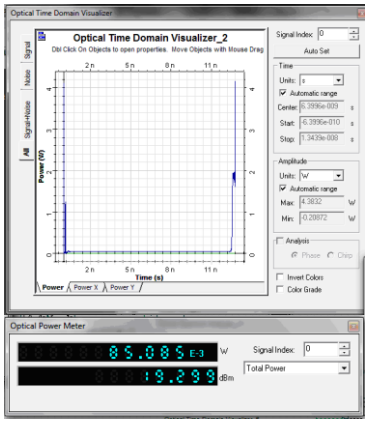

Fig 7: Time domain visualizer and optical power meter output at A=1 and B=1

Truth table obtained from the time domain analysis and power meter outputs corresponding to input signals are as below.

1. TABLE I: Truth table of Optical NAND gate

S.No.	A	B	Output Power(W)	Output power (dB)	Logic
1	0	0	595.888e-3	27.752	1
2	0	1	595.772e-3	27.751	1
3	1	0	596.015e-3	27.752	1
4	1	1	85.085e-3	19.299	0

From above truth table it is clear that the output is high when any of the input bit is low. So we can conclude that it is a truth table of NAND gate.

B. Design and simulation of Optical NOR gate

In the design of Optical NOR gate two data pumps (A and B) which can carry data signals and a probe pump (CW Laser) is used to generate the logic of NOR gate. The output of two data pumps are coupled together by the first coupler to get a logic of OR gate i.e the output will be high when any one of the input is high, this output is coupled with probe pump by second coupler and the output of this second coupler is fed to the SOA. Now three signals of different frequency is given as input to the SOA, these input signals will generate the FWM signal when any two inputs signal are high. When any of transmitter (data pump) is at logic '1' it will generate the FWM signal with probe pump (CW laser). The power of each data pump and probe pump is coupled together, When FWM signal is generated it spreads the power of CW laser and if we filter the signal of CW laser by BPF (tuned at the frequency of probe pump), a lower value of power will be obtained which can be considered a logic '0'. When both the data pumps are at logic '0' no FWM signal will be there at the output of SOA, so the total power of CW laser will be there at the output of BPF and it can be considered as logic

'1'. The signal of CW laser is selected by first BPF and amplified; this amplified signal is again passed through the second BPF with the center frequency of CW laser to remove the unwanted signals.

The frequencies of data pumps and probe pump are taken as below.

f_A = 193THz, f_B = 193.1THz, $f_{CW\ laser}$ = 192.9

When both the inputs are high i.e logical input given to the transmitter A and B is logic "1", FWM is generated at output of SOA as shown in figure 8. FWM is showing the spread of total power at different peaks.

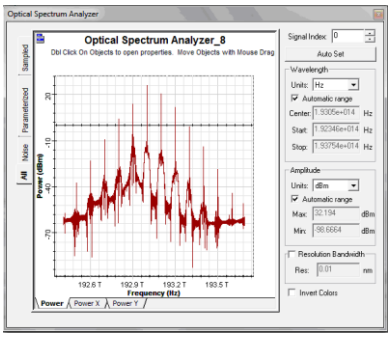

Fig 8: Spectrum analyzer at output of SOA (FWM Generation) when both inputs are high

Since the BPF is set at the frequency of CW laser i.e at 192.9THz, it will pass only one peak corresponding to CW laser which is below the threshold level because total power of CW laser is used to generate number of peaks as shown in fig 10 and is detected as '0'. If only one data pump is high, it will again generate the FWM signal with CW laser and a lower value of output power will be obtained.

When the input bit given at the bit sequence generator of both the transmitter is '0' then there will be no optical signal at the output of first coupler and at the second coupler only the optical power corresponding to CW laser will be obtained. The output of second coupler is given as input to the SOA. So the peak corresponding to only CW laser is obtained, which is then filtered by BPF with the center frequency of 192.9 THz and amplified. This amplified signal is again filtered to remove the unwanted signals. Since the total power of CW laser is taken at output, it will generate logic '1' at the output, as shown in fig 9.

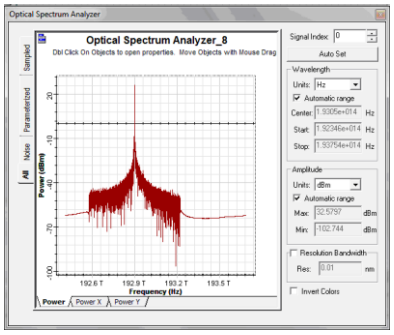

Fig 9: Spectrum analysis at the output of SOA when both inputs are zero

For output power calculation time domain visualizer and power meter is used for different combination of input sequences as shown in figure 10-13.

1. A=0 and B=0

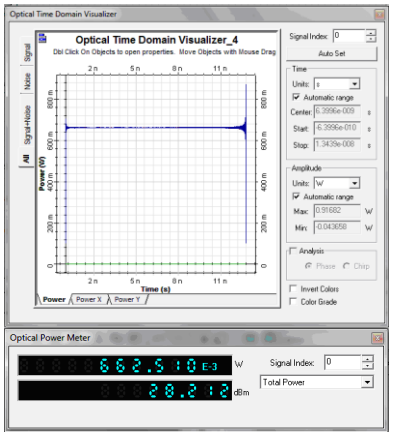

Fig 10: Output of time domain visualizer and power meter at A=0 and B=0

2. A=0 and B=1

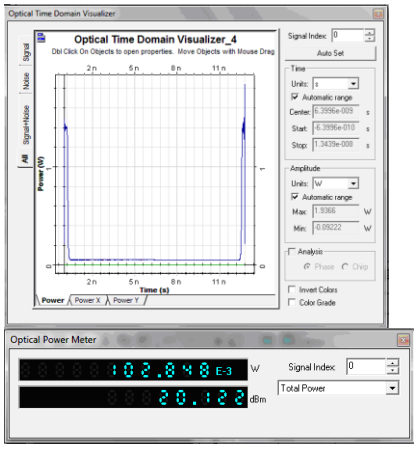

Fig 11: Output of time domain visualizer and power meter at A=0, B=1

3. A=1 and B=0

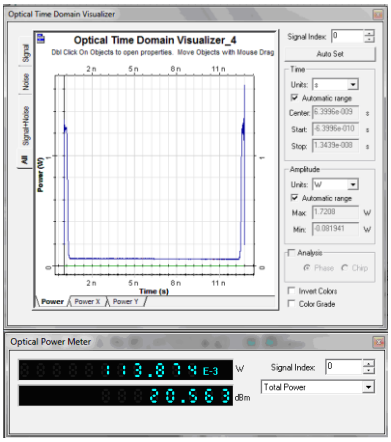

Fig 12: Output of time domain visualizer and power meter at A=1, B=0

4. A=1 and B=1

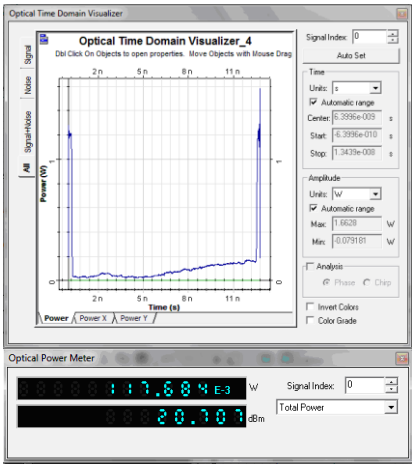

Fig 13: Output of time domain visualizer and power meter at

Above results are corresponding to different logical inputs, so to generate the logic at the output, truth table is prepared as follows

2. TABLE II: Truth table for optical NOR gate

S.No.	A	B	Output Power(W)	Output power (dB)	Logic
1	0	0	662.510e-3	28.212	1
2	0	1	102.848e-3	20.122	0
3	1	0	113.874e-3	20.563	0
4	1	1	117.684e-3	20.707	0

From above truth table we can see that the output power is low when any of the input bit is high, so we conclude that the output power is corresponding to a logic of NOR gate.

III. Conclusion

In conclusion, we have numerically simulated all-optical logic gates NOR and NAND gates at 40 Gb/s. In order to optimize the extinction ratio and output power for the two logic levels various parameters such as input optical power, SOA active length region and SOA current gain has been varied. Being universal logic gate these gates can be used for designing many switching and storage devices. Hence these gates can be the key elements in next-generation optical networks and computing systems to perform optical signal processing functions such as all-optical label swapping[5], wavelength converter, header recognition[6][7], parity checking, binary addition, and data encryption.

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