A 11.8mW Low Noise Amplifier for 3-8GHz Wideband Application

Dilip I. Thakor[1] and Prof. Pankaj P. Prajapati[2]

[1]**Electronics and Communication Engg. Department, Gujarat Technological University,**
L. D. College of Engineering, Ahmedabad, Gujarat, India.
dilipthakor022@gmail.com

[2]**Electronics and Communication Engg. Department Gujarat Technological University,**
L. D. College of Engineering, Ahmedabad, Gujarat, India.
pp12479@yahoo.co.in

Abstract

This paper deals with the design of wideband CMOS low-noise amplifier (LNA) that combines a narrowband LNA topology with a resistive shunt feedback. The resistive shunt feedback provides wideband input matching by reducing the Q-factor of the narrowband LNA input and flattens the gain. The output peaking network is designed using bridged-shunt-series peaking network to achieve bandwidth extension. The proposed wideband amplifier is implemented in 0.13-µm CMOS technology for a 3-8GHz UWB system. Simulation is performed using the SPICE software and the BSIMV3 model for the 0.13-µm CMOS process. The measured gain is greater than 16dB and the noise spectral density of -180 to -188dB. The total power consumption of the wideband low-noise amplifier is 11.8mW.

Keywords: *CMOS, feedback, low noise amplifier (LNA), peaking, bandwidth extension.*

1. Introduction

Ultra wideband radio, potentially offers higher communication speeds than traditional narrowband transceivers. The advantage of the UWB transceiver over narrowband systems is low cost, low power, and high data rate due to the large bandwidth. A significant difference between traditional radio transmission and UWB radio transmission is that traditional communications systems transmit data by varying the power level, frequency, and/or phase of a sinusoidal wave. However, in UWB radio, data is transmitted either as impulse radio (IR) or multiband orthogonal frequency division multiplex (OFDM). The IR UWB transmits data based on the transmission of very short pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. This technique results in lower data rate and lower design complexity compared to the OFDM system. On the other hand, in the multiband OFDM technique each band with 528 MHz width encodes the data using QPSK modulation. Using this technique a data rate of 480 Mb/s can be achieved. However, the design of this system is more challenging. One of the major challenges in wideband communications systems is the design of a wideband low-noise amplifier (LNA). As the first active component in the receiver chain, the LNA should offer sufficient gain and low noise to keep the overall receiver noise figure as low as possible. In most applications, it is desirable to obtain wideband on-chip input matching to a 50Ω antenna/filter, good linearity, and low power consumption. In addition, gain-flatness over the entire frequency range of interest is necessary to meet the design specifications. Among wideband designs, distributed and common-gate amplifiers suffers from high noise figure. Additionally, cascading of several stages degrades the linearity of the LNA [5]-[6].

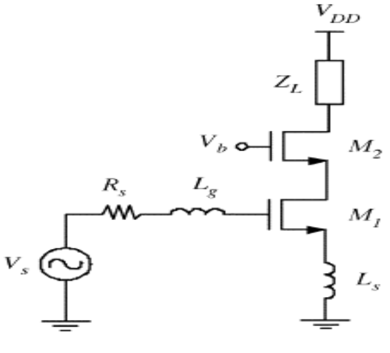


Figure 1.Source inductor degenerated LNA.

This paper introduces the source inductor degeneration with resistive feedback topology to achieve wideband input matching and the bridge-shunt-series peaking network to achieve the wideband output response. In bridge-shunt-series peaking network, better bandwidth extension ratio (BWER) is achieved using capacitive splitting-an inductor is inserted to separate the total load capacitance into two constituent components [1].

2. Wideband LNA Design

Figure 1 shows the source inductor degenerated LNA topology. In figure 1, the inductor *Ls* is added for simultaneous noise and input matching and L_g for the impedance matching between the source resistance R_s and the input of LNA [7]. A proposed Wideband LNA design can be achieved by using the resistive feedback topology with narrowband LNA design as shown in figure 2(a). This feedback amplifier consisting of a cascade transistor pair M_1 and M_2 as shown in figure 2(a). Capacitor C_F blocks the DC voltage to the gate of the M_1. The bias voltage V_{bias} provides DC bias for the input transistor M_1. The bias voltage V_{bias} can be generated by designing the voltage divider using CMOS [10]. The cascade transistor improves the isolation and reduces the Miller capacitance while the voltage gain of input transistor M_1 should be small. Inductor L_g performs series resonance with C_{gs} of M_1 for input impedance matching.

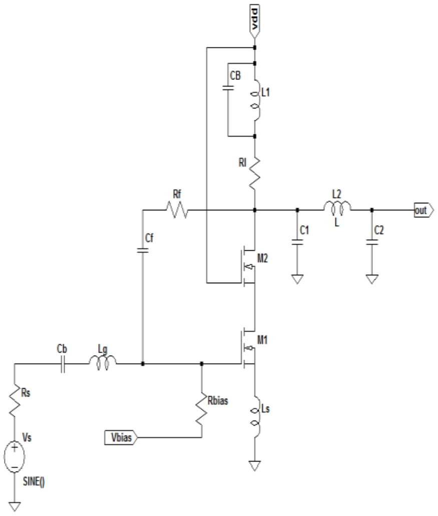
$$\omega_t = \frac{R_s}{L_s} = \frac{g_{m1}}{C_{gs1}} \tag{1}$$

$$L_s = \frac{1}{\omega_0{}^2 C_{gs}} - L_g \tag{2}$$

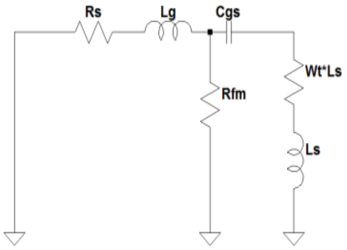
To broaden 3 dB bandwidth, the LNA employs the bridged-shunt-series peaking network as shown in figure 2(a) and to achieve wideband output matching source follower buffer can be designed. Figure 2(b) shows the small-signal equivalent circuit for the input part of the proposed wideband LNA. In Fig. 2(b), the resistor $R_{fm} = [R_f /(1\text{-}A_v)]$ represents the Miller equivalent input resistance of R_f , where A_v is the open loop gain of the LNA. From figure 2(a) and (b), the value of R_f can be much larger than the conventional resistive shunt feedback. However, in the proposed topology input impedance is determined by $\omega_T L_s$. The important role of the R_f is to reduce the Q-factor of the circuit. The Q-factor of the circuit in figure 2(b) is given by

$$Q_{wb} \approx \frac{1}{\left[R_s + \omega_t L_s + \dfrac{(\omega_0 L_g)^2}{R_{fm}}\right]\omega_0 C_{gs}} \tag{3}$$

Equitation (3) indicates that by properly selecting the value of the feedback resistor R_f, small value of Q-factor can be achieved. The bandwidth is inversely proportional to the Q-factor of the circuit so, wide bandwidth can be achieved.



(a)



(b)

Figure 2 Proposed Wideband LNA. (a) Schematic, (b) small-signal equivalent circuit at the input.

For $R_f >> R_s$, $R_f >> R_l$ and $g_m R_f >> 1$, the noise factor of the amplifier is given by

$$F > 1 + \frac{R_s}{R_f}\left[1 + \frac{1}{g_{m1}R_s}\right]^2 + \frac{\gamma}{g_{m1}R_s} \tag{4}$$

Where γ = 2 for short channel technique. From equation (3) and (4), it can be seen that the feedback resistor R_f is the key component to get the tradeoff between gain and noise figure. From above all equations components values are calculated, which are shown in table 1.

Table 1
List of Component Values of Wideband LNA

Components	Values
L_s	0.14nH
L_g	2nH
L_1	3.5nH
L_2	4.2nH
R_f	800Ω
C_f	2pF
$(W/L)_1$	260/0.13
$(W/L)_2$	200/0.13
R_l	50Ω

3. Simulation Results

The CMOS wideband LNA with resistive feedback topology and bridge-shunt-series peaking network is designed using 0.13-µm CMOS technology. The supply voltage V_{dd} is 1.2V. The proposed LNA design is simulated using the SPICE software. Figure 3 shows the simulated gain of designed wideband LNA. As shown in figure 3, the gain at 3.2GHz is 25 dB which is maximum. At 5GHz, the measured gain is 17dB (min.). So, the proposed design of LNA provides Gain more than 16dB over the entire range of 3-8GHz. Noise performance of the proposed LNA can be achieved in terms of Noise spectral density. Figure 4 (a), (b) shows the simulated noise spectral density in volts and dB's, respectively. The proposed LNA design provides the noise spectral density of -180dB to -188dB. From noise spectral density noise figure is calculated, which is 2.6dB (min) achieved. Figure 5 shows the power response of the proposed LNA design. The power consumption of the proposed LNA is 11.8mW. Table 2 summarizes the performance of proposed LNA.

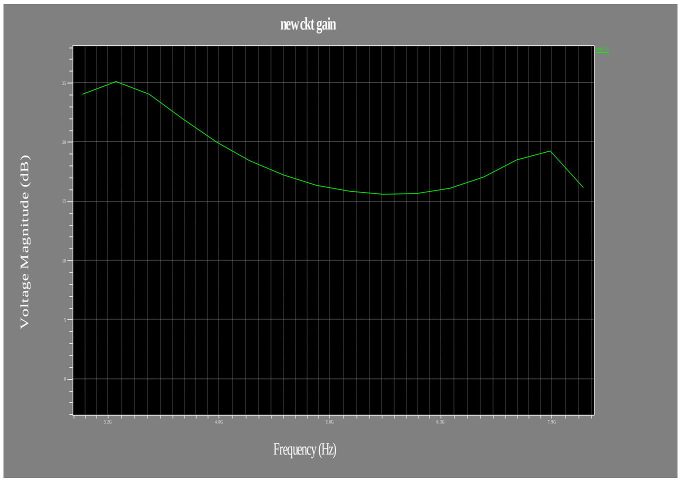
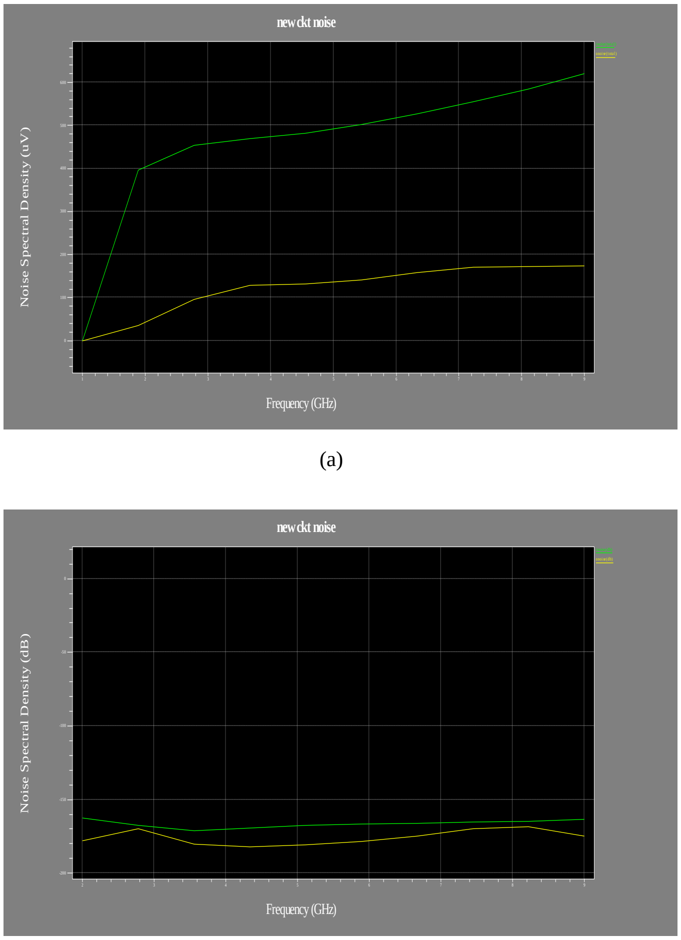


Figure 3. Simulated gain response of proposed LNA.



(a)

(b)

Figure 4. Simulated noise spectral density in (a) µv, (b) dB.

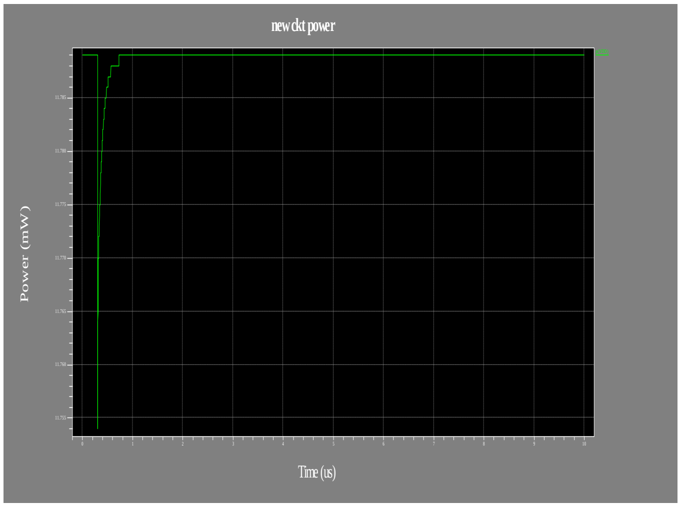


Figure 5. Simulated power response of proposed LNA.

Table 2
Performance Summary

Technology	0.13-µm CMOS
Supply voltage	1.2v
Frequency	3-8GHz
Gain	>16dB
Noise spectral density	-188dB (min)
Noise Figure	2.6dB (min)
Power consumption	11.8mW

4. Conclusion

A compact wideband LNA has been designed in 0.13-µm CMOS technology for wideband and low power application. The proposed LNA design uses the resistive shunt feedback topology with inductor degeneration topology. At the output side bandwidth can be extended using bridge-shunt-series network by dividing the load capacitance in two components. The amplifier achieved a bandwidth more than 5GHz, a gain more than 16dB and better noise performance with lower power consumption.

References

[1] S. Shekhar, J. S. Walling, and D. J. Allslot, "Bandwidth Extension Techniques for CMOS Amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, Nov. 2006.

[2] Ke-Hou Chen, Jian-Hou Lu, Bo-Jiun Chen and Shen-Iuan Liu, "An Ultra Wide Band 0.4-10 GHz LNA in 0.18-µm CMOS*," IEEE Trans. Circuits Syst. II: Express briefs*, vol. 54, no.3, March 2007.

[3] Yi-Jing Lin, Shawn S. H. Hsu, Member IEEE, Jun-De Jin and C. Y. Chan, "A 3.1-10.6 GHz Ultra Wideband CMOS Low Noise Amplifier With Current Reused Technique," *IEEE Microwave and Wireless Components Letters*, vol. 17, nO. 3, March 2007.

[4] Qiang Li, Member, IEEE, and Yue Ping Zhang, "A 1.5 V 2-9.6 GHz Inductor-less Low Noise Amplifier in 0.13-µm CMOS," *IEEE Trans. Microwave Theory and Techniques*, vol. 55, no. 10, Oct. 2007.

[5] A. Meaamar, C. C. Boon, M. A. Do, and K. S. Yeo, "A 3–8 GHz lownoise CMOS amplifier," *IEEE Microw.Wireless Components Lett.*, vol. 19, no. 4, pp. 245–247, Apr. 2009.

[6] K. H. Chen and C. K. Wang, "A 3.1-10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for UWB Application," *IEEE Asia-Pacific Conference on Advanced System Integrated Circuits*, August 2004.

[7] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, "An ultra-wideband CMOS low noise amplifier for 3-5 GHz UWB system*," IEEE J. Solid-State Circuits*, vol. 40, no.2, pp. 544-547., Feb. 2005.

[8] Kambiz Moez and M. I. Elmastry, "A Low-Noise CMOS Distributed Amplifier for Ultra-Wide-Band Applications," *IEEE Trans. Circuits and Systems II*, vol. 55, no. 2, Feb. 2008.

[9] Bosco Leung, VLSI for Wireless Communication, Prentice Hall Electronics and VLSI Series, pp. 75-89.

[10] B. Razavi, Design of Analog Integrated CMOS Circuits, Mc-Graw Hill, 2001.

Dilip Thakor received his B.E. (Electronics and communication) degree from Vishwakarma Government Engineering College, Gujarat University, Chandkheda in 2007. He has two year Industrial work experience. Currently he is pursuing Masters in Communication Systems Engineering at L.D. College of Engineering under Gujarat Technological University.

Prof. Pankaj Prajapati received his B.E. degree in Electronics and Communication engeering from L. D. college of Engeering in 2001 and the M. Tech. (VLSI Design) from Nirma University in 2009. He has 8 years of teaching experience in this field. Since June 2011, he is working as Assistant Professor at L. D. College of Engineering.