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Design Optimization of Memristor Based 6T and 7T SRAM Cells using Sleep transistor at Nanoscale Techniques

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Abstract

The factors which affect the need of low power design is the rising of leakage current, scaling of technologies and large power dissipation in high performance computing systems. Due to aggressive scaling of devices, leakage current is increasing to an inevitable extent and the efforts have been made to propose an optimized circuit to reduce the power consumption. In this paper, we have proposed a 6T Memristor based SRAM and 7T Memristor based SRAM by employing sleep transistor stacking technique. The outcome has resulted in optimization of leakage current and power dissipation by 16.82% and 45% respectively. At 45 nm technologies, impact of process parameter variations largely affects the proposed circuit. In this paper, the effects and remedies of process parameter variations have also been discussed, explored and elaborated. The results have been validated and compared with the standard results. The simulation results have been carried out in Cadence Virtuoso 45nm technology.

Keywords: Memristor, 6T SRAM, 7T SRAM and Sleep Transistor.

1. Introduction

SRAM stands for Static Random Access Memory. SRAM is a volatile memory which can store data till the power is on and as the power supply gets OFF, the stored data cannot be retained. Memory cell of SRAM is the latch or flip-flop i.e. in the form of inverters. It is used to store the value given in the form of input. SRAMs are available in different types of technologies like bipolar and MOS technologies, although various applications use SRAMs made up of NMOS or SRAMs made of CMOS technology [1]. As we know that BJTs which are Bipolar in nature are fast in operation. They have the plus point of speed whereas the MOS related devices have much greater capacities and lower power consumption[2].They are commonly used as the internal memory of a computer. The CPU continually performs read and write operations on this memory at a very fast rate. The memory chips that are interfaced to the CPU have to be therefore, fast enough to be compatible with the CPU commands. Every device has its own speed of operation, but to have proper functioning and synchronization it is necessary to match the commands of CPU[3,4].Today's requirement while designing any electronic device is small or compact size and high performance or high speed operation. SRAMs fulfill this requirement. Many microprocessors controlled instruments and appliances have very small memory capacity requirements [5]. Some instruments such as digital storage oscilloscopes and logic analyzers require very high speed memory. For such applications, SRAMs are normally used. In this paper we have discussed why 7TSRAM is better than 6TSRAM and why the sleep technique used SRAM is better than the simple one [6]. It is observed through parameters like leakage current, voltage and total transient power. It was found after the calculations that all the above mentioned parameters were reduced in the bit cell sleep technique employed SRAMs.

2. Memristor

Unlike the conventional two terminal device like capacitor, inductor Memristor is a device that exhibits non-volatile property and retention characteristic that are worthy of storing data that are stable[7,8,9].It can be used as a two terminal device and if needed as a three terminal device also. To make Memristor three terminal device, one transistor is used in one of the terminals of memristor with its gate terminal as sel (select). Drain is connected to one of the terminals and the other end is grounded. When current flows into the thick line of memristor symbol, resistance of the device decreases and when current flows out of the thick black line, resistance of the device increases. Based on these actions of resistances, memristors are able to perform different logic operations.

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Memristors give the functional relationship between magnetic flux and electric charge [10, 22]

$$f(\Phi_m(t), q(t)) = 0 \quad (1)$$

Where, Φ_m is defined as the magnetic flux linkage and is defined as the integral of voltage over time. Mathematically[11] it is represented as

$$M(q) = d\Phi m / dq \quad (2)$$

$$M(q(t)) = (d\Phi m / dt)/(dq/dt) = V(t)/I(t) \quad (3)$$

As shown in the above equations, memristor is associated with both magnetic flux linkage and charge its unit becomes W_b per C or ohms. It shows all the fundamental elements namely resistor, capacitor, inductor and the fourth missing element that was discovered by Leon O. Chua in the year 1971[12]. Next is the symbol of fourth element Memristor with i/o terminals.

3. 6T SRAM Operation

6T Memristor based SRAM is the generic SRAM cell. It requires six transistors per bit.To start the operation of cell, word line is asserted or enabled. It has two inverters that are cross coupled with two transistors M5 and M6 that are further connected to bit lines BL and BLB. M5 and M6, also termed as Pass transistors, are controlled by the Word Line (WL).

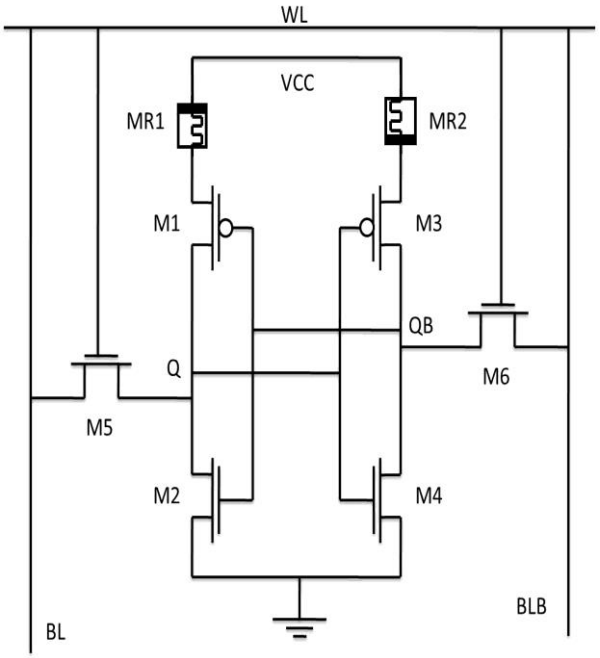

Fig.1. 6T Memristor based SRAM cell

6T Memristor based SRAM has three operation states namely write, read and hold. As mentioned earlier, M5 and M6 transistors are controlled by the Word Line (WL) which indicate that the word line decides whether the operation is hold or read or write. If WL is zero (WL = 0), the operation is HOLD and if WL is one (WL = 1), the operation is either READ or WRITE.

In HOLD operation, the word line is not asserted It is made to be equal to zero (WL = 0). As a result, the pass transistors are OFF and the data is held in the latch.

In WRITE operation, word line is asserted and is made equal to one (WL = 1), as a result of which the pass transistors are ON and the new data or the new value or the new voltage applied to BL and BLB is overwritten in the latch[13].

In READ operation, WL = 1 so M5 and M6 transistors are ON. Both the BL and BLB bits lines are pre charged to logic 1. Values stored in Q and QB are transferred to the bit lines by leaving BL to its pre-charged value and discharging BLB to logic 0[14].

4. 7T SRAM Operation

7T Memristor based SRAM is composed of two CMOS inverters cross-coupled to each other with pass transistors that are further connected with the bit lines BL and BLB. In addition to this 7TSRAM has one extra NMOS transistor connected to word line. An extra NMOS transistor N5 is used for the feedback connection and disconnection[15].

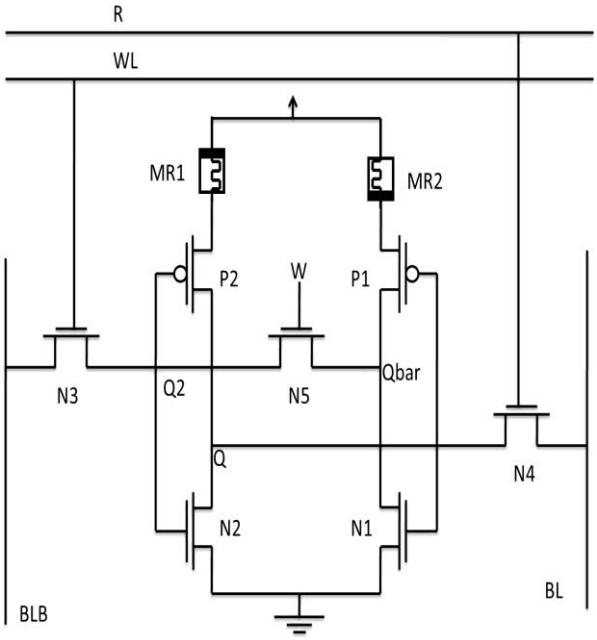

Fig.2. 7T Memristor based SRAM cell

In WRITE operation, N5 is turned OFF. As a result, feedback connection gets OFF and SRAM cell behaves like two cascaded inverters; inverter 2 followed by inverter 1. When some value is assigned at the input, BLB carries the complement of that assigned value which is transferred

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to drive the inverter 1. To write zero (0), BLB is kept one (1) and to write one (1), BLB is kept zero (0) [16].
In READ operation, N5 is turned ON and in this mode, the cell behaves like conventional 6TSRAM cell. Both BL and BLB are pre-charged high before and after the read and write operation[17].

5. Sleep Transistor Technique

The technique used in this paper is sleep technique. The need of using this technique arises from the fact that as the technologies are being scaled down, leakage current is becoming a limitation which is stated clearly in ITRS. As the successive technologies are scaled down to 180nm, 90nm, 45nm and so on, the channel length is reducing. As a result, gate oxide thickness and threshold voltage is also changing and is scaled down, which affects the leakage current,this in term also impact the power dissipation[18,19] of the circuit. As we know that, power dissipation is given as:

$$P_D = C\,(V_D)^2 F \quad (4)$$

where, C is the capacitance, V_D is the power supply and F is the switching frequency.
Leakage power is given by;

$$P_L = I_L . V_D \quad (5)$$

where, I_L is the leakage current and V_D is the power supply.

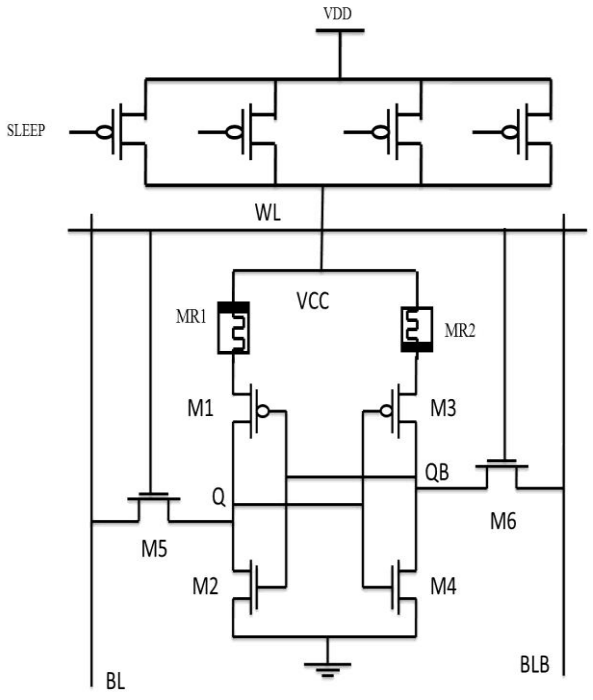

Fig.4. Sleep Technique employed 6T Memristor based SRAM

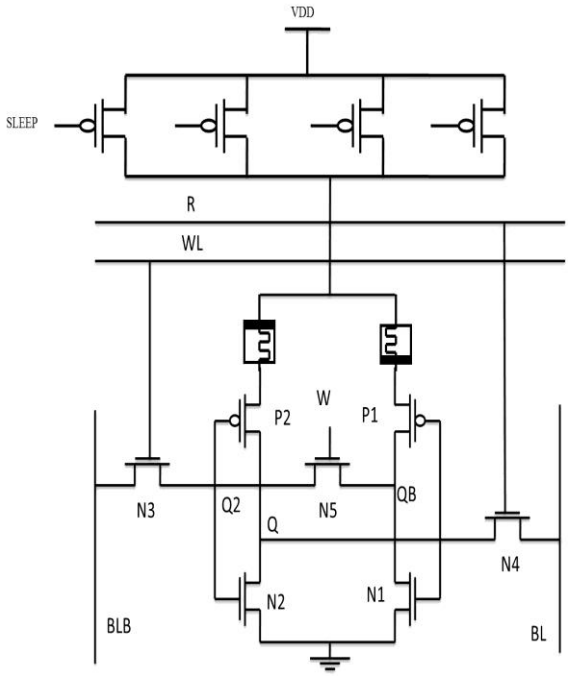

Fig.5. Sleep Technique employed 7T Memristor based SRAM

Hence, if we are able to minimize this leakage current, power leakage can also be minimized to a great extent and hence this technique of sleep is used. So bit cell sleep technique[1] is used to minimize the gate leakage current which is a high threshold voltage transistor that can be either PMOS or NMOS[20,21].

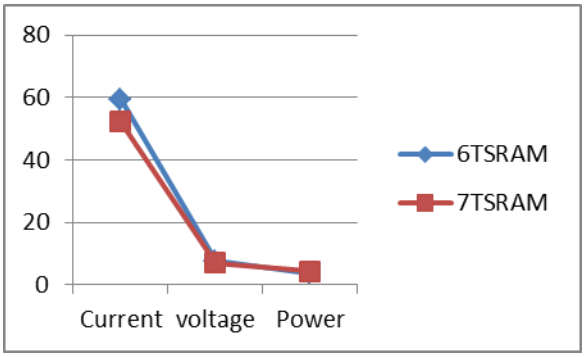

Fig.7. Sleep technique employed SRAM representing leakage parameter; leakage current in (pA), voltage in (mV), power in (nA)

Conclusions

This SRAM based paper brings forth the design of simple Memristor based 6TSRAM, 7TSRAM and sleep technique employed 6TSRAM, 7TSRAM in 45nm technology. By observing the graphs and the tabular contents, it is evident that 7T SRAM is better than the 6T SRAM and the sleep technique employed 7T SRAM is better than the 6TSRAM

due to the reduction in leakage parameters and effective power consumption. The proposed technique reduces the gate leakage current which is one of the main factors influencing the performance of SRAM due to the scaling of technologies. It is also found that the power consumed by the sleep technique SRAMs is less when compared with the simple SRAMs. This verifies the objective of this paper that the technique employed SRAMs are better than the simple SRAMs.

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