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Rail to Rail Operational Amplifier for Sample & Hold Circuit in Pipeline ADC

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Abstract

The papers presents a 1V rail to rail operational amplifier that has been used as a unity gain buffer in the sample and hold circuit for 1V 10 bit 1Msps pipeline ADC in 0.18µm technology. An open loop architecture is chosen for the implementation of sample and hold circuit. The transmission gate switch is used in the sample and hold circuit for reducing the effect of channel charge injection and clock feed through. Also, the transmission gate switch offers a low resistance as compared to pMOS or nMOS switches switches. The sample and hold circuit speed up to 1Msps has been achieved.

Keywords: *Rail to Rail,SNR, amplifier ADC.*

1.Introduction

Sample and Hold circuits are heart of any Analog to Digital Converter and is used to improve the dynamic performance of the ADCs. Unity gain buffers are used to implement sample and hold circuits. With the increasing demand for the low power battery operated systems, the unity gain buffers need to be designed at low supply voltage but the voltage headroom available is limited at low supply voltages so noise starts dominating over the signal thereby reducing signal-to-noise ratio (SNR) as well as the dynamic range of the sample and hold circuits. At higher supply, this is not a problem because the signal range is high as compared to noise. Therefore, to improve SNR rail to rail signal swing is required at the input as well as at the output of unity gain buffer at low voltages[1].

2. Proposed Circuit for Rail to Rail Operation

The proposed circuit for getting rail to rail operation using input CM adapter circuit is shown in Fig.1. In this, two pairs of extra transistors ML1-ML2 and ML3-ML4 are used to make the current flow through the resistors to close the feedback loop. The idea behind this is to make transistor ML1-ML4 work only when the voltage dependent current source transistors M10-M13 are off.

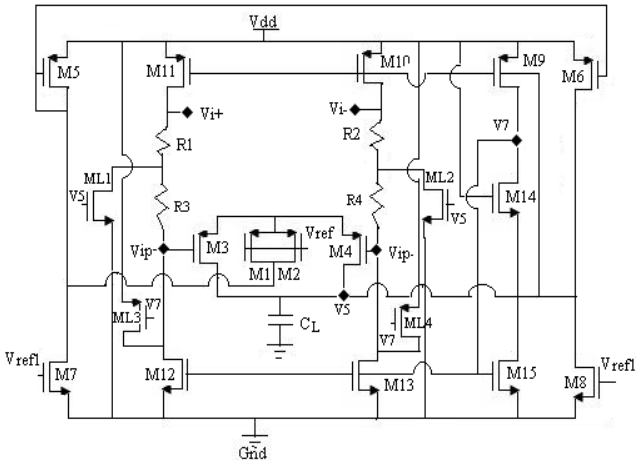

Fig.1. Proposed Circuit for rail to rail operation

When the input common mode voltage is lower than Vref, then the current sources are off because V5 and V7 are sufficiently high and low respectively but these are utilized to turn on ML1-ML2 and ML3-ML4 respectively at the same time. As soon as the input common mode voltage exceed Vref, the voltage V5 and V7 become low and high enough to turn on M10-M13 transistors and turn off the transistor ML1-ML4. Therefore, the circuit works in its usual manner for Vi,cm greater than Vref and extra transistor pairs come into action when Vi,cm becomes lower than Vref. The Transistor ML1-ML2 pair is designed to provide a low resistance path to ground.

The resistors used in the earlier circuit is modified and divided into two unequal half. A sufficiently high value of resistor R1, R2 is selected in order to avoid the current flow into the input node and a low value of resistors R3-R4 is used. In this way, the output voltage is fixed to Vref for the whole common mode range[2].

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3. Sample and Hold Circuit Design

A Simple open loop sample and hold architecture has been chosen as shown in Fig.2. It consists of a transmission gate switch Mn-Mp pair, sampling capacitor Ch and a unity gain buffer. Transmission gate switch instead of pass transistor switch is chosen to reduce the effect of channel charge injection and clock feedthrough. Vin and Vout are the input and output voltage signals of the sample and hold circuit and clock signal controls the transmission gate switch. The sample and hold circuit is designed for 1V 10-bit 1Msps Pipeline ADC[3].

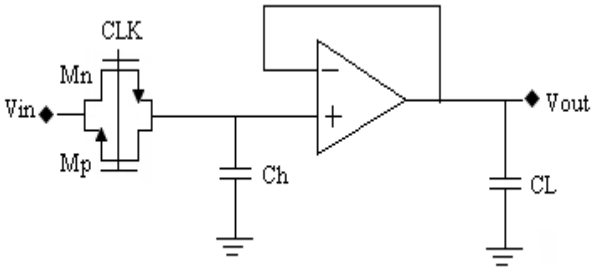

Fig.2. Open Loop Sample and Hold Circuit

3.1 Design Considerations:

3.1a Selection of Sampling Capacitor

The sampling capacitor plays an important role in deciding the signal to noise ratio (SNR) since in sample and hold circuit the maximum rms sampling noise isKTCh. So, a high value of sampling capacitor is desired in order to have a good SNR but high value of sampling capacitor means the sampling period will also become high thereby reducing the speed of the circuit. Thus a optimum value of capacitor is chosen which satisfy both the above requirements.

3.1b Selection of Transmission gate Resistance

Once the sampling capacitor value is determined, the transmission gate resistance (Rx) can be found out from the time constant specification. As this is a simple RC sampling circuit, the time constant(τ) can be written as:

$\tau = RxCh$

$Rx = \tau Ch$

3.2 Buffer Design Requirements:

3.2a Slew Rate

Slew rate is determined from the ability to charge the load capacitor to the full scale voltage (Vpp) within the time allocated for slewing (Ts/8). As a rule of thumb, the time allocated for slewing should be ¼ of half the sampling period (Ts/8)[3]. Therefore, slew rate can be calculated as:

$$\text{Slew Rate} \geq (Vpp\ Ts8)$$
$$\geq 8 * VppTs$$

So, for Vpp =0.8 volts and Ts = 1µs

Slew Rate≥6.4 V/µs

3.2b Unity Gain Bandwidth

As the slewing time is Ts/8 so the remaining sampling time 3Ts/8 is used for the small signal settling. The settling time determines the unity gain bandwidth from the following formula:

Unity Gain Bandwidth $UGB \geq \ln 2N + 12\pi\beta tsettling$

For N= 10 bits, tsettling=375 ns

Therefore, UGB≥3.23 MHz

Also,

$UGB = gm1,2/(2\pi CL)$

This relation also gives the same UGB as derived using settling time constraint.

3.2c DC Gain

The DC gain is calculated on the basis of error allowed for sample and hold circuit for a given resolution. The error that can be tolerated for an N-bit ADC is expressed as[4]:

error $eo < 2N+1$

N=10 gives

$eo < 2\text{-}11$

Now, The DC gain can be calculated using the formula below:

$eo = 11 + Ao\beta$

Therefore, Open Loop Dc Gain Ao≥66.22 dB

3.2d Tail Current and Transconductance

The tail current is determined from the slew rate specification. Thus, for a given slew rate, tail current source can be determined as:

ItailCm≥6.4 V/µs

Therefore,

Itail≥5.12 µA

4.Simulation Results

The complete circuit has been simulated using 0.18µm BSIM 3v3.1 Model parameters in 0.18µm technology. In the frequency response curve, the dashed line shows the phase curve while the solid line represents gain of the amplifier.

4.1 Complete Operational Amplifier

Parameters	Notation Used	Units	Value
Process	-----	µm	0.18
Supply Voltage	Vdd	V	1
Gain	Ao	dB	93.567
Slew Rate	SR	V/µs	8.946
Phase Margin	PM	degrees	61.396º
Unity Gain Bandwidth	UGB	MHz	14.9445

Common Mode Rejection Ratio	CMRR	dB	139.8
Power Supply Rejection Ratio	PSRR	dB	85.32
Input Common Mode Range	ICMR	V	0-1
Output Common Mode Range	OCMR	V	0.046-0.95
Power Dissipation	PD	µW	175.01

Table 1: Specifications of Complete rail to rail Operational amplifier

4.2Sample and Hold Circuit

Parameter	Notation Used	units	Value
Resistance	R	kΩ	1.1
Hold Capacitor	Ch	pF	10
Sampling Speed	Fs	MHz	1
Input signal range	ISR	V	0-1
Output Signal Range	OSR	V	0.046-0.95

Table2: Specifications of the Sample and Hold Circuit

Fig.3 & 4 gives the positive and negative slew rates of the complete rail to rail Operational amplifier. The positive and negative slew rates obtained are 8.4 V/µs and 12.2 V/µs respectively for a tail current of 11.88µA.

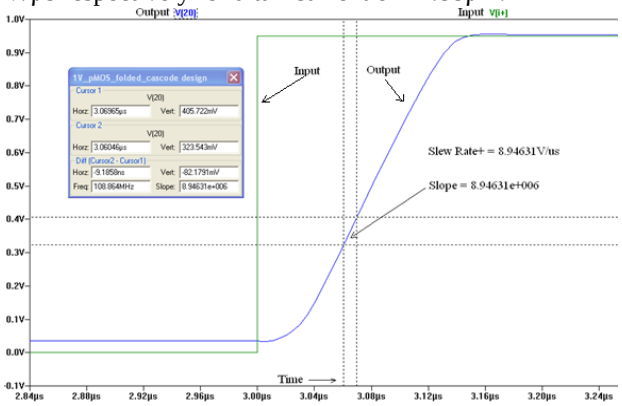

Figure3: Positive Slew rate of rail to rail Op-amp

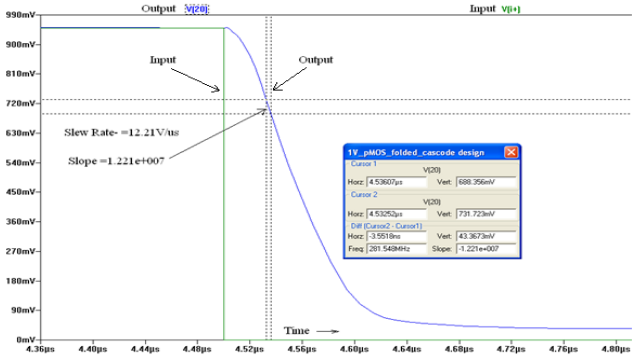

Figure4: Negative Slew rate of rail to rail Op-amp

Fig.5& 6 shows the transient response of the the complete rail to rail Operational amplifier connected in unity gain configuration. A sinusoidal response of the unity gain buffer is shown in Fig.11 for 0.84 Vpp.

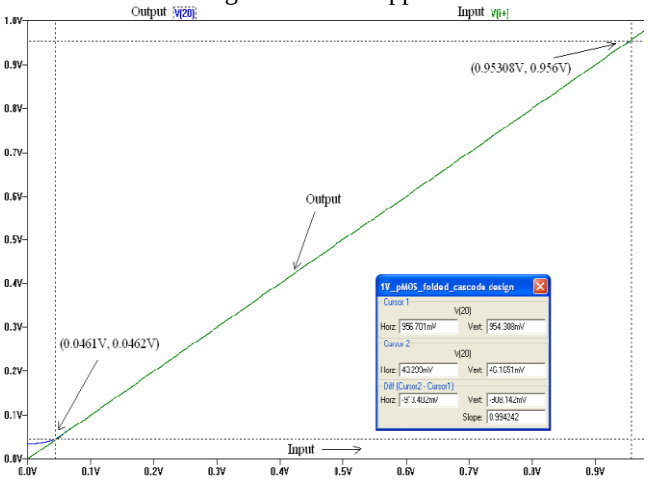

Fig.5 Transient response of a rail to rail Op-amp connected in unity gain configuration

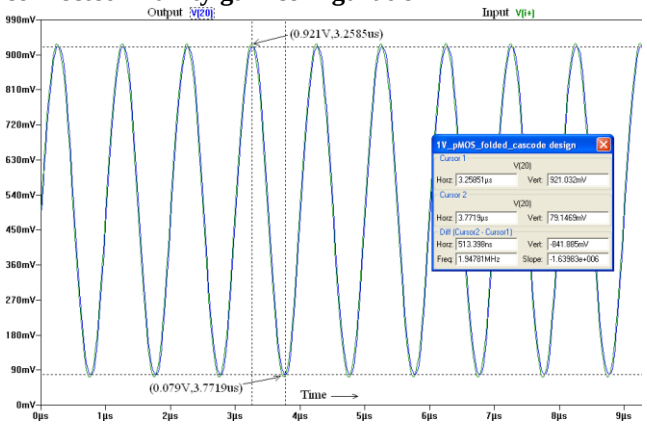

Fig.6 Transient response of a rail to rail Op-amp connected in unity gain configuration for sinusoidal signal of 0.84 Vpp

Fig.7 shows the sample and hold output with respect to the ramp input applied. The clock frequency of 1MHz with a sampling capacitor of 10pF is achieved.

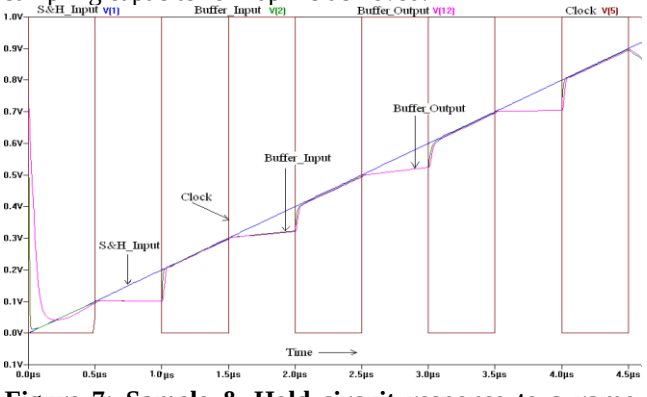

Figure 7: Sample & Hold circuit response to a ramp input signal.

5. Conclusion

The paper deals with designing a rail to rail amplifier. The paper presents a 1V rail to rail operational amplifier that can be used as a unity gain buffer in the sample and hold circuit for 1V 10 bit 1Msps pipeline ADC in 0.18µm technology. A low voltage rail to rail Operational amplifier using the single differential pair employing the dynamic level shifting technique has been designed in 0.18µm technology.The Operational amplifier has been designed to achieve high speed by employing extra bias circuitry for high slew rate. This amplifier has been used successfully as a unity gain buffer in the design of sample and hold circuit for use in pipeline ADC having 10 bit resolution and a speed of 1 Msps speed.

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