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An Power Efficient New CRT Based Reverse Converter for Moduli Set $\{2^n+1, 2^n-1, 2^{2n}, 2^{2n+1}-1\}$

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Abstract

The 4-moduli$\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$ set has been recently proposed for large dynamic range of 6n-bits .for this 4-moduli set reverse converter design based on New CRT-1 and MRC has already been proposed. In this paper we propose reverse converter design for 4-moduli set$\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$based on New CRT-II theorem to achieve more efficient residue number system(RNS) than the former one. The design is achieved using carry save adders and carry propagate adders only i.e. it is purely adder based. We implemented the proposed reverse converter design on a standard 180nm CMOS technology and when compared with the other equivalent state of art converters it has indicated about 34% better performance in terms of power.

Keywords-*Residue Number system (RNS) , Chinese Remainder Theorem (CRT) , Mixed Radix Conversion (MRC) , New Chinese Remainder Theorems (NEW CRTS) , Reverse converter .*

1. Introduction

In recent years RNS has been considered as an interesting topic in research field of DSP applications. RNS is an alternative to the conventional number system where the absence of carry propagation between arithmetic units conveys its importance[1].RNS provides high speed and parallel computations which leads to its successful application in the additions and multiplication subjugated high speed DSP applications such as digital filters, convolutions [2][3],fast Fourier transforms, digital communications[4],computer arithmetic[5],digital image processing and the like[6].

An RNS consists of three major components : a forward converter for converting conventional weighted number to residue representation, an arithmetic unit module consisting of modulo adder, multipliers, an reverse converter for converting residues into its equivalent conventional weighted number representation.[7]

For efficient and lucrative RNS implementation moduli set selection and reverse conversion are the two most critical issues. Moduli set selection is an important issue since the complexity and speed of resulting conversion structure depends on chosen moduli set. The selection of an appropriate conversion algorithm for the reverse conversion design is a critical issue for efficient design of RNS. Several conversion techniques have been proposed based on CRT, MRC, and New CRTs.[8]

Recently many large dynamic range moduli sets have been introduced such as
$\{2^n-1, 2^{2n}, 2^{2n+1}-1\}$[9] ,
$\{2^n-1, 2^{2n}, 2^n+1, 2^{2n}+1\}$ [10],
$\{2^{2n}-1, 2^{2n}, 2^{2n}+1\}$ [11],$\{2^{2n+1}-1, 2^{2n+1}, 2^{2n}-1\}$[12].
The 4-moduli set $\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$ was proposed in [13] .The moduli set has been implemented using mixed combination of New CRT-I theorem and MRC in [13] and with only MRC in [14] .The major advantage of this moduli set is its simpler implementation which can lead to fast RNS arithmetic unit.

In this paper we propose reverse conversion design for the moduli set based on new Chinese remainder theorem-II .the design is achieved using carry save adders and carry propagate adders only .the architecture is designed without the use of multiplier and ROMs i.e. it is memory less and adder based implementation .When compared with the other state of art converters the proposed design has indicated about 34% better performance in terms of power.

The rest of paper is structured as follows Section 2 provides brief background on reverse conversion method. The proposed reverse converters design for the moduli set along with hardware implementation is presented in Section 3 .the performance of the reverse converter design is analyzed and evaluated in Section 4 and it is followed by conclusion in Section 5.

2. Back ground

Residue Number System (RNS): An RNS can be defined in terms of a relatively-prime moduli set $\{M_1, M_2, \ldots, M_n\}$ where gcd(M_i, M_j) = 1 for i ≠ j and gcd(a, b) denotes the greatest common divisor of a and b. A weighted number X can be represented as X = ($x_1, x_2, \ldots, x_n$), where

$$x_i = X \bmod M_i = |X|_{M_i},\ 0 \le x_i < M_i \quad (1)$$

Such a representation is unique for any integer X in the range [0,M-1], where M=$M_1, M_2, \ldots, M_n$ is the DR of the moduli set $\{M_1, M_2, \ldots, M_n\}$ [1].

New Chinese Reminder Theorem –II*:* Using CRT-II with four moduli set $\{M_1, M_2, M_3, M_4\}$, the number X can be calculated from its corresponding residues (x_1, x_2, x_3, x_4) using the following equations

$$X = Z + M_1 M_2 |k_1 (Y - Z)|_{M_3 M_4} \quad (2)$$

$$Z = x_1 + M_1 |k_2 (x_2 - x_1)|_{M_2} \quad (3)$$

$$Y = x_3 + M_3|k_3(x_4 - x_3)|_{M_4} \quad (4)$$

Where

$$|k_1 x M_1 x M_2|_{M_3M_4} = 1 \quad (5)$$

$$|k_2 x M_1|_{M_2} = 1 \quad (6)$$

$$|k_3 x M_3|_{M_4} = 1 \quad (7)$$

Where k_1, k_2, k_3 are the multiplicative inverses[15].

3.PROPOSED REVERSE CONVERTER DESIGN

In this section New CRT-II technique is applied to the moduli set $\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$ hardware implementation of the conversion technique is also presented.

The following properties are required for the derivation of residue to binary converter and used for further simplification to decrease hardware complexity.

Property 1*:* Modulo(2^p-1) multiplication of a residue number by2^k, where p and k are positive integers, is equivalent to k bit circular left shifting.

Property 2*:* A negative number in modulo (2^p-1) is equivalent to the one's compliment of the number, which is obtained by subtracting the number from (2^p-1).

Theorem 1*:* For the moduli set $\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$, the following holds true:

$$|((2^{2n+1}-1)(2^{2n}))^{-1}|_{2^{2n}-1} = 2^{2n+1}-1 \quad (8)$$

Therefore $k_1 = 2^{2n+1}-1$

$$|(2^{2n})^{-1}|_{2^{2n+1}-1} = 2^{2n+1}+1 \quad (9)$$

Therefore $k_2 = 2^{2n+1}+1$

$$|(2^n+1)^{-1}|_{2^n-1} = 2^{n-1} \quad (10)$$

Therefore $k_3 = 2^{n-1}$

Proof*:* If it can be demonstrated that $|(2^{2n+1}-1)\times(2^{2n})\times(2^{2n+1}-1)|_{2^{2n}-1} = 1$, then $2^{2n+1}-1$ is the multiplicative inverse of $((2^{2n+1}-1)(2^{2n}))$ with respect to $2^{2n}-1$.$|(2^{2n+1}-1)\times(2^{2n})\times(2^{2n+1}-1)|_{2^{2n}-1}$is given by $|1\times1\times1|_{2^{2n}-1}$ = 1.Thus Eq (8) holds true and $k_1 = 2^{2n+1}-1$ .In the same way $|(2^{2n})\times(2^{2n+1}+1)|_{2^{2n+1}-1} = 1$, thus $2^{2n+1}+1$ is multiplicative inverse of $(2^{2n+1}+1)$ with respect to $2^{2n+1}-1$.it is given by $|\frac{1}{2}\times 2|_{2^{2n+1}-1} = 1$.Therefore Eq (9) holds true and hence$k_2 = 2^{2n+1}+1$.

Similarly $|(2^{n-1})\times(2^n+1)|_{2^n-1} = 1$, thus 2^{n-1} is multiplicative inverse of (2^n+1) with respect to 2^n-1.it is given by $|\frac{1}{2}\times 2|_{2^n-1} = 1$ .Therefore Eq (10) holds true and $k_3 = 2^{n-1}$

Theorem 2: For the given three moduli set $\{M_1, M_2, M_3, M_4\}$ = $\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$,the number X can be derived from its corresponding residues (x_1, x_2, x_3, x_4) by

$$X = Z + (2^{2n})(2^{2n+1}-1)|(2^{2n+1}-1)(Y-Z)|_{2^{2n}-1} \quad (11)$$

$$Z = x_1 + 2^{2n}|2^{2n+1}+1(x_2-x_1)|_{2^{2n+1}-1} \quad (12)$$

$$Y = x_3 + 2^n+1|2^{n-1}(x_4-x_3)|_{2^n-1} \quad (13)$$

By substituting $M_1 = 2^{2n}$, $M_2 = 2^{2n+1}-1$, $M_3 = 2^n+1$, $M_4 = 2^n-1$ and values of k_1, k_2, k_3 from theorem 1 into Eq (2)-(4) we get Eq (11)-(13).

Consider moduli set $\{2^{2n}, 2^{2n+1}-1, 2^n+1, 2^n-1\}$,with corresponding residues (x_1, x_2, x_3, x_4), let the binary representations of the residues be :

$$x_1 = x_{1,2n-1} \dots\dots\dots\dots\dots\dots x_{1,0} \quad (14)$$

$$x_2 = x_{2,2n} \dots\dots\dots\dots\dots\dots x_{2,0} \quad (15)$$

$$x_3 = x_{3,n} \dots\dots\dots\dots\dots\dots x_{3,0} \quad (16)$$

$$x_4 = x_{4,n-1} \dots\dots\dots\dots\dots\dots x_{4,0} \quad (17)$$

From Eq (11) we get

$$Z = x_1 + 2^{2n}A \quad (18)$$

Where

$$A = |(2^{2n}+1)(x_2-x_1)|_{2^{2n+1}-1} = |(2^1)(x_2-x_1)|_{2^{2n+1}-1} = |v_1+v_2|_{2^{2n+1}-1} \quad (19)$$

$$v_1 = |(2^1)x_2|_{2^{2n+1}-1} = |(2^1)x_{2,2n} \dots\dots\dots x_{2,0}|_{2^{2n+1}-1} = \underbrace{x_{2,2n-1} \dots\dots\dots x_{2,0}x_{2,2n}}_{2n+1} \quad (20)$$

$$v_2 = |-(2^1)x_1|_{2^{2n+1}-1} = |-(2^1)(0x_{1,2n-1} \dots\dots x_{1,0})|_{2^{2n+1}-1} = \underbrace{\bar{x}_{1,2n-1} \dots\dots\dots \bar{x}_{1,0}1}_{2n+1} \quad (21)$$

Next

$$Y = x_3 + (2^{2n}+1)B \quad (22)$$

Where

$$B = |(2^{n-1})(x_4-x_3)|_{2^n-1} = |v_3+v_4|_{2^n-1} \quad (23)$$

$$v_3 = |(2^{n-1})x_4|_{2^n-1} = |(2^{n-1})x_{4,n-1} \dots\dots\dots x_{4,0}|_{2^n-1} = \underbrace{x_{4,0}x_{4,n-1} \dots\dots\dots x_{4,1}}_{n} \quad (24)$$

$$v_4 = |(-2^{n-1})x_3|_{2^n-1} = |(-2^{n-1})x_{3,n} \dots\dots\dots x_{3,0}|_{2^n-1}$$

$$= |(-2^{n-1})(2^n \times x_{3,n}) + (x_{3,n-1} \dots\dots\dots x_{3,0})|_{2^n-1} \quad (25)$$

$$v_4' = |(-2^{n-1})x_{3,n-1} \dots\dots\dots x_{3,0}|_{2^n-1} = \underbrace{\bar{x}_{3,0}\bar{x}_{3,n-1} \dots\dots\dots \bar{x}_{3,1}}_{n} \quad (26)$$

$$v_4'' = |(-2^{n-1})(2^n \times x_{3,n})|_{2^n-1} = |(-2^{n-1}) \times 2^n(\underbrace{0 \dots\dots 0}_{n-1}x_{3,n})|_{2^n-1} = \bar{x}_{3,n}\underbrace{1 \dots\dots 1}_{n-1} = 0\underbrace{1 \dots\dots 1}_{n-1} \quad (27)$$

Since x_3 , is a number that is smaller than 2^{n+1} ,we can consider two cases for x_3 . First, when $x_3$is smaller than 2^n, and thesecond, when x_3 is equal to 2^n .

Therefore we have

$$v_4 = \begin{cases} v_4' \text{if } x_{3,n} = 0 \\ v_4'' \text{ if } x_{3,n} = 1 \end{cases} \quad (28)$$

Next

$$X = Z + 2^{2n}(2^{2n+1} - 1)\,|(2^{2n+1} - 1)(Y - Z)|_{2^{2n}-1}$$
$$X = Z + 2^{2n}(2^{2n+1} - 1)\,C \quad (29)$$

Where

$$C = |(2^{2n+1} - 1)(Y - Z)|_{2^{2n}-1} = |(Y - Z)|_{2^{2n}-1}$$
$$= |(x_3 + (2^{2n} + 1)B - x_1 - 2^{2n}A)|_{2^{2n}-1}$$
$$= |(v_5 + v_6 + v_7 + v_8)|_{2^{2n}-1} \quad (30)$$

$$v_5 = |(x_3)|_{2^{2n}-1} = |(x_{3,n} \dots\dots x_{3,0})|_{2^{2n}-1} = \underbrace{x_{3,n} \dots\dots\dots x_{3,0}}_{2n} \quad (31)$$

$$v_6 = |(2^{2n} + 1)B|_{2^{2n}-1} = |(2^{2n} + 1)\underbrace{B_{n-1} \dots B_0}_{n}|_{2^{2n}-1}$$
$$= \underbrace{B_{n-1} \dots B_0}_{n}\,\underbrace{B_{n-1} \dots B_0}_{n} \quad (32)$$

$$v_7 = |(-x_1)|_{2^{2n}-1} = |-(x_{1,2n-1} \dots x_{1,0})|_{2^{2n}-1}$$
$$= \underbrace{\bar{x}_{1,2n-1} \dots\dots \bar{x}_{1,0}}_{2n} \quad (33)$$

$$v_8 = |(-2^{2n}A)|_{2^{2n}-1} = |(-2^{2n})\underbrace{A_{2n} \dots A_0}_{2n+1}|_{2^{2n}-1}$$
$$= |(-2^{2n}) \times 2^{2n} \times A_{2n}) + \underbrace{(A_{2n-1} \dots A_0)}_{2n}|_{2^n-1} \quad (34)$$

$$v_8' = |(-2^{2n})A_{2n-1} \dots\dots A_0|_{2^n-1} = \underbrace{\bar{A}_{2n-1} \dots\dots \bar{A}_0}_{2n} \quad (35)$$

$$v_8'' = |(-2^{2n})(2^{2n} \times A_{2n})|_{2^n-1}$$
$$= |(-2^{2n}) \times (\underbrace{0 \dots 0}_{2n-1} A_{2n})|_{2^n-1}$$
$$= \underbrace{1 \dots 1}_{2n-1}\bar{A}_{2n} \quad (36)$$

Hence

$$C = |(v_5 + v_6 + v_7 + v_8' + v_8'')|_{2^{2n}-1} \quad (37)$$

then

$$X = Z + 2^{2n}(2^{2n+1} - 1)\,C$$
$$= x_1 + 2^{2n}A + 2^{2n}(2^{2n+1} - 1)\,C$$
$$= x_1 + 2^{2n}(A + (2^{2n+1} - 1)\,C)$$
$$= x_1 + 2^{2n}D \quad (38)$$

Where

$$D = A + (2^{2n+1} - 1)\,C = E - C \quad (39)$$
$$E = A + (2^{2n+1})C = \underbrace{C_{2n-1} \dots C_0}_{2n}\underbrace{A_{2n} \dots A_0}_{2n+1} \quad (40)$$

Then

$$X = x_1 + 2^{2n}D = \underbrace{D_{4n} \dots D_0}_{4n+1}\underbrace{x_{1,2n-1} \dots x_{1,0}}_{2n} \quad (41)$$

Hardware implementation:

The hardware structure of the proposed reverse converter is shown in Fig.1. Implementation is based on Eq (18), Eq (19), Eq (22), Eq (23), Eq (29), Eq (37), Eq (39), Eq (40) and Eq (41).The operand preparation unit prepares the required operands in equations Eq (20), Eq (21), Eq (24), Eq (26) and Eq (27) by simple manipulation of the routing of the bits of residues. We require (6n+3) Not gates for performing the inversions in Eq (15), Eq (19) and Eq (20).

The operand 'A' and 'B' are obtained by using 2n+1-bit and n-bit Carry Propagate Adders (CPAs) with End Around Carry(EAC) respectively. The operand preparation unit-2 prepares the required operands in Eq (31)-(36) by simple manipulation of the routing of the bits of residues .For the five operands $(v_5, v_6, v_7, v_8', v_8'')$it requires three levels of 2n-bit Carry Save Adders(CSA) with End Around Carry(EAC) followed by a 2n bit Carry Propagate Adder(CPA) with End Around Carry (EAC). The computation of equation (38) it requires another operand preparation unit-3 for obtaining 'E' by just concatenation of (2n+1) bits of A with 2n bits of C. Next a (4n+1)-bit Carry Propagate Adder(CPA) with End Around Carry (EAC) is used to obtain 'D'. Finally the computation of Eq (41) requires just concatenation of (2n) bits of x_1 with 4n+1 bits of 'D'. The description of different parts of the proposed reverse converter is given in Table 1.

Table 1
Hardware requirements of proposed converter

Parts	FA	Not	Xor/and Parts	Xnor/or parts	Mux 2x1	Delay
OPU1	-	*2n*	-	-	*1(n)-bit*	$T_{mux} + t_{not}$
CPA1	*2n*	-	-	*1*	-	$(4n+2)t_{FA}$
CPA2	*n*	-	-	-	-	$(2n)t_{FA}$
OPU2	-	*4n+1*	-	-	-	t_{NOT}
CSA1	*n+1*	-	*n-1*	-	-	t_{FA}
CSA2	*1*	-	-	*2n-1*	-	t_{FA}
CSA3	*2n*	-	-	-	-	t_{FA}
CPA3	*2n*	-	-	-	-	$(4n)t_{FA}$
OPU3	-	*2n*	-	-	-	t_{NOT}
CPA4	*2n*	-	-	*2n+1*	-	$(4n+1)t_{FA}$

4. PERFORMANCE EVALUATION

The performance of the proposed reverse converter is evaluated by performing both theoretical and practical analysis by implementing it using application specific integrated circuit. The results of theoretical analysis are presented in Table 2. This table suggests that in terms of area, delay the proposed Reverse converter based on New CRT-II is on par with the other backward converters.

In order to perform an accurate comparison and analysis, all the converters are described in Verilog HDL and simulated with ISEv14.3.All the conversion circuits are implemented using cadence RTL compiler. The converters are implemented using 180nm standard cell technology libraries of TSMC.

The practical results presented in Table-3 for n=6,8,10,12 and 16 suggests that proposed reverse converter achieved about 34% power reduction over the other reverse converters in the same class of 6n-dynamic range. The efficiency of the proposed converter is much better with increase in the value of 'n'. The area and delay of the proposed converter when compared with converter in [13], it shows slight better performance of 6% and 7% respectively.

The practically analysis of the proposed converter suggests that in aspects of Area x Power, Power x Delay and Area x Power x

Delay, it is capable of 38.52%, 38% and 42% better performance respectively over the equivalent state of art converters.

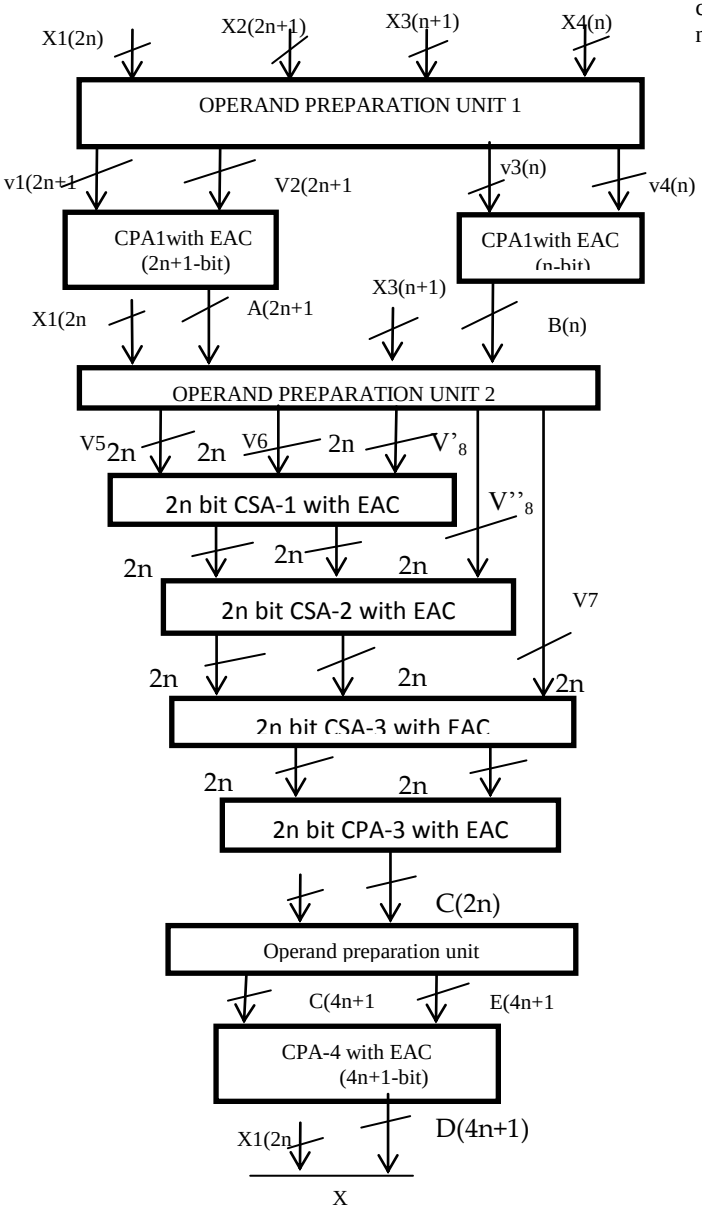

Fig.1. Hardware Architecture of Proposed Converter

4. Conclusion

In this paper we proposed a reverse converter design based on New CRT-II for 4-moduli set . The proposed backward converter is memory less and purely adder based. Hardware architecture of the proposed converter employs only Carry Save Adders (CSAs) and Carry Propagate Adders (CPAs).

The performance of the proposed converter is evaluated both theoretically and practically. The experimental results suggests that proposed reverse converter is 34% better in terms of power when compared to the converter in [13]. Further, in aspects of Area x Power, Power x Delay and Area x Power x Delay, it is capable of 38.52%, 38% and 42% better performance respectively over the other equivalent state of art converters. Performance will be much better for large values of n.

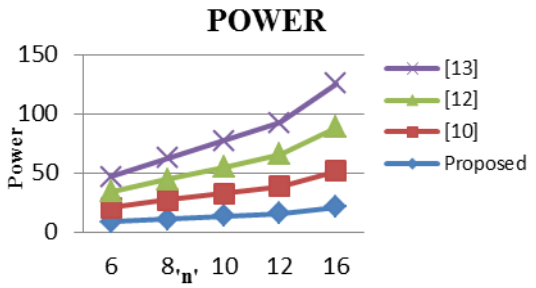

Fig .2.Power comparison of converters

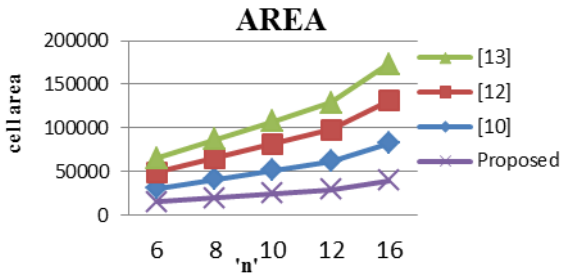

Fig .3.Area comparison of converters

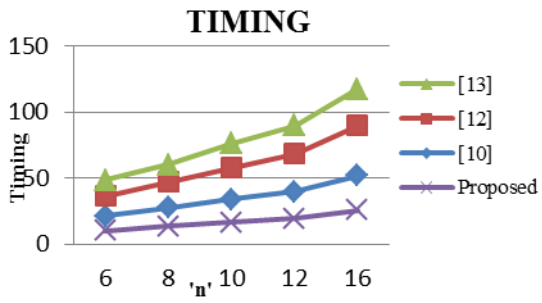

Fig .4 .Delay comparison of converters

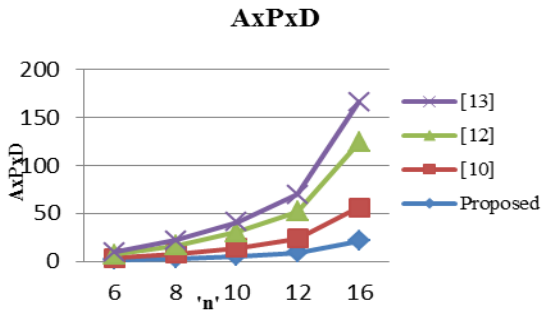

Fig .5.Area x Power x Delay comparison of converters

TABLE 2
HARDWARE REQUIREMENTS AND CONVERSION DELAYS OF THE DIFFERENT REVERSE CONVERTERS

Moduli set	**Area**	**Delay**
[10]	$(10n+6)A_{FA}+(4n-3)A_{XOR}+(4n-3)A_{AND}+(2n-3)A_{XNOR}+(2n-3)A_{OR}+(6n+3)A_{NOT}$	$(8n+3)t_{FA}+t_{NOT}$
[12]	$(8n+3)A_{FA}+(4n-2)A_{XNOR}+(4n-2)A_{OR}+(6n+1)A_{NOT}$	$(4n+6)t_{FA}+t_{NOT}$
[13]	$(10n+3)A_{FA}+(n+1)A_{XOR}+(n+1)A_{AND}+(3n-1)A_{XNOR}+(3n-1)A_{OR}+(7n+3)A_{NOT}$	$(12n+6)t_{FA}+2t_{NOT}$
PROPOSED	$(10n+2)A_{FA}+(n-1)A_{XOR}+(n-1)A_{AND}+(4n+1)A_{XNOR}+(4n+1)A_{OR}+(n)$ 2×1mux $+(8n+1)A_{NOT}$	$(14n+3)t_{FA}+t_{MUX}+3t_{NOT}$

TABLE 3
AREA, POWER, DELAY RESULTS FOR PROPOSED AND OTHER BACKWARD CONVERTERS
For n=6

Moduli set	**Cell Area (μm^2)**	**Power($nW\times10^5$)**	**Delay(ns)**	**Area × Power ($\mu m^2\times nW\times10^9$)**	**Power ×Delay ($nW\times ns\times10^7$)**	**Area × Power ×Delay ($\mu m^2\times nW\times ns\times10^{11}$)**
[10]	19234	15.7	13.03	3.01	2.04	3.93
[12]	22543	16.7	17.43	3.76	2.91	6.56
[13]	15680	12.58	12.15	1.97	1.51	2.37
PROPOSED	19328	8.48	10.21	1.27	0.86	1.29

For n=8

Moduli set	**Cell Area (μm^2)**	**Power($nW\times10^5$)**	**Delay(ns)**	**Area × Power ($\mu m^2\times nW\times10^{10}$)**	**Power ×Delay ($nW\times ns\times10^7$)**	**Area × Power ×Delay ($\mu m^2\times nW\times ns\times10^{11}$)**
[10]	21349	16.12	14.08	3.44	2.27	4.84
[12]	24463	17.58	19.47	4.30	3.42	8.37
[13]	20871	17.63	15.12	3.67	2.66	5.56
PROPOSED	21468	10.66	13.27	2.12	1.41	2.81

For n=10

Moduli set	**Cell Area (μm^2)**	**Power($nW\times10^5$)**	**Delay(ns)**	**Area × Power ($\mu m^2\times nW\times10^{10}$)**	**Power ×Delay ($nW\times ns\times10^7$)**	**Area × Power ×Delay ($\mu m^2\times nW\times ns\times10^{11}$)**
[10]	26680	18.91	17.16	5.04	3.24	8.65
[12]	26796	22.25	24.12	6.78	5.36	16.34
[13]	26005	22.49	18.21	5.84	4.09	10.64
PROPOSED	30470	13.45	16.35	3.32	2.19	5.42

For n=12

Moduli set	**Cell Area (μm^2)**	**Power($nW\times10^5$)**	**Delay(ns)**	**Area × Power ($\mu m^2\times nW\times10^{10}$)**	**Power ×Delay ($nW\times ns\times10^7$)**	**Area × Power ×Delay ($\mu m^2\times nW\times ns\times10^{11}$)**
[10]	37369	27.37	23.32	10.22	6.38	23.85
[12]	42483	32.25	33.32	13.7	10.75	45.67
[13]	31196	26.59	21.28	8.29	5.65	17.65
PROPOSED	37532	15.45	19.43	4.56	3.01	8.86

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