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# Asymmetric SRAM- Power Dissipation and Delay

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**Abstract**

In recent years rapid growth is noticed in mobile, hand-held communication devices, battery operated devices and fast data transfer demand, that these systems should have larger memory capacity and low power consumption with minimum operational delays. Since memory is main and consisting a large part of systems, nearly fifty percent, reducing the power and delay in memories becomes a hot burning issue. Almost half of the total CPU (central processing unit) dissipation is due to memory operations. It is necessary to identify the sources of power consumption and delay in memory blocks so that they can be reduced, hence allowing for better overall performance of the system. Today's microprocessors are very fast and require fast caches with low power dissipation and low delay. This paper presents the simulation results of 6T SRAM (six transistors static random access memory) cells, which are the main choice for today's cache applications. The stability of the cell is best among all the cells, existing in memory cell configurations.

***Key words:*** *static random access memory, power dissipation, simulation.*

## 1. Introduction:

Fast and low power SRAMs have become a critical component of many VLSI chips (very large scale integration). This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory [1,12]. Simultaneously, power dissipation has become an important consideration due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances [16]. While process [3-5] and supply [4,10,13] scaling remain the biggest drivers of fast low power designs. This paper investigates dissipation in power and delay which can be used in conjunction for scaling to achieve fast and low power operations.

### 1.1 Asymmetric Cell Technique

Structure of the cell is identical to the 6T symmetric SRAM cell. The difference lies in the dual threshold voltages of the PMOS and NMOS transistors. When the supply voltage is gradually brought down, the transistor threshold voltage is also varied to maintain performance [11]. As a result of the low threshold voltage, leakage power increases rapidly due to the exponential relationship between leakage and Vt. Leakage can be reduced by using higher-V*t* transistors, but it will result in reduced leakage while maintaining performance comparable to traditional cells. SRAM cell designs that lead to new cache designs, which we refer to asymmetric-cell caches (ACC) as shown below in figure1. ACCs exploit the fact that, in ordinary programs, most of the bits in caches are zeroes for both the data and instruction streams [8] and all caches are not utilized at the same time.

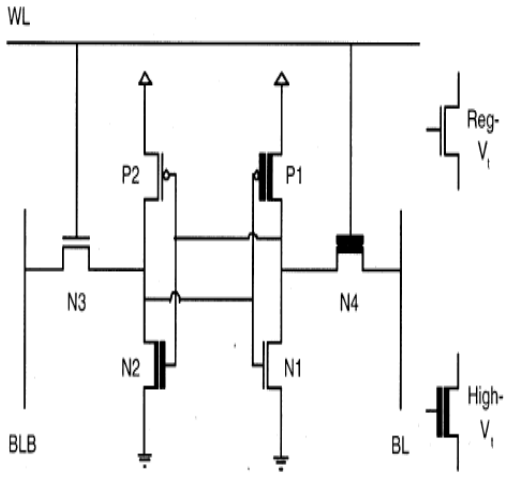


Figure 1: Asymmetric 6T SRAM cell.

It has been shown that this behavior persists for a variety of programs under different assumptions about cache sizes, organization, and instruction set architectures, even when

perfect knowledge of which cache parts will be left unused for long periods of time is known beforehand [6]. The asymmetrical cell family is built on the following premise: select a preferred stored value and weaken, by increasing the threshold voltage, only those transistors necessary to drastically reduce leakage when this value is stored [18].

## 2. Sources of Power Dissipation

2.1 Dynamic power dissipation

Dynamic power dissipation is further classifies into two categories, namely short circuit power and power consumption during switching.

2.1.1 Short circuit power:

As if the input signals are having finite slopes which causes direct-path currents to flow through the gate for a short time during switching operation. For this short duration of time, there exists a direct path between $V_{DD}$ and GND and circuit consumes large amount of power [12].

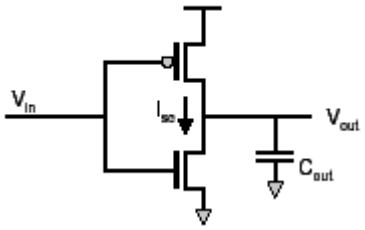


Fig: 2: Short Circuit Power Dissipation

From the figure 2 the energy consumed per switching is calculated as below

$$E_{dp} = V_{dd} * I_{Peak} * t_{sc} \quad \text{..... (1)}$$

$$P_{shortcut} = V_{dd} * I_{peak} \quad \text{..... (2)}$$

Where
$V_{dd}$ = Voltage supply
Ipeak = Peak current
$t_{sc}$ = time period of power consumption

Matching the rise and fall times of the gate will results in reduced short circuit power. In practice, however, the times are not matched, since optimizing for propagation delay can result in unmatched times. So circuit power is also a major source of power consumption in the digital circuits [2,15].

2.1.2 Power Consumption during Switching

Charge is moved from $V_{dd}$ to the output of the inverter, during and after input transaction, hereby pulling $V_{out}$ to $V_{dd}$. The lumped capacitance $C_L$ results from parasitic wire capacitances and from gate capacitances of the logic gates driven by the inverter, which is shown in figure 3.

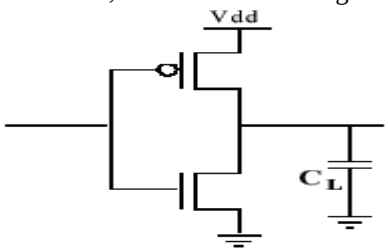


Fig: 3: Dynamic Power Dissipation

Upon the opposite transition of the input, the PMOS transistor switches off and the NMOS transistor switches on. Now the charge stored on $C_L$ is moved to ground. This output capacitances consumed the power during switching is known as the dynamic power dissipation. It is the largest source of energy dissipation in CMOS circuits [7, 9, 17]. In summary, one rising and the following falling transition of the output consume energy of: -

$$E = C_{Load} * V_{dd} * V_{dd} \quad \text{.....(3)}$$

Where
$C_{Load}$ is the load capacitance
$V_{dd}$ is the Power supply

If f is the clock frequency and the average number of low to high or high to low transitions (the switching activity) of the node is denoted by $\alpha$ then the power consumption due to capacitive switching is given by:

$$P_{switching} = \alpha C_{Load} (V_{dd})^2 f \quad \text{.....(4)}$$

Where
$\alpha$ = activity factor
$V_{dd}$ = voltage swing of the output node
$C_{Load}$ = effective capacitance of the output load
f = switching frequency

2.2 Static Power Dissipation

Traditionally, the static component of power consumption has been negligible in static CMOS. But as mentioned in the introduction, this is no longer the case. A number of Leakage mechanisms begin to gain significance. Most of these mechanisms are directly or indirectly due to the small device geometries [6, 7, 9, 14].

(a) $\mathbf{I_{rev}}$ is called reverse bias p-n junction leakage.

(b) $\mathbf{I_{sub}}$ is the subthreshold leakage current.
(c) $\mathbf{I_{gate}}$ is the gate oxide tunneling.
(d) $\mathbf{I_{hot}}$ is the gate current.
(e) $\mathbf{I_{GIDL}}$ is gate induced drain leakage.
(f) $\mathbf{I_{PT}}$ channel punch through leakage

### 2.3 Subthreshold Channel Leakage

The second source of leakage current is the subthreshold leakage through a MOS device channel. Even though a transistor is logically turned off, there is a non-zero leakage current, through the channel at the microscopic level. This current is known as the subthreshold leakage because it occurs when the gate voltage is below its threshold voltage. Leakage current is given as follows:

$$I_{subth} = A * e^{\frac{q}{nkT}(V_{GS} - V_t)} \left(1 - e^{\frac{qV_{DS}}{kT}}\right) \quad \ldots\ldots (5)$$

It can be seen directly from the equation that the subthreshold leakage current is less if $V_t$ is more and vice versa. Therefore asymmetric configuration deals with dual threshold voltage in each SRAM cell [7, 9, 17].

## 3. Simulation results and discussion:

Table 1: Power Dissipation and Delay of 6T ASRAM cell

| Operation | Power Dissipation (watts) | Delay (ns) |
|---|---|---|
| Stand by | $7.109 \times 10^{-7}$ | 10 |
| Write Operation | $3.447 \times 10^{-11}$ | 0.1 |
| Read Operation | $9.122 \times 10^{-10}$ | 0.1 |

### 3.1 Standby Condition

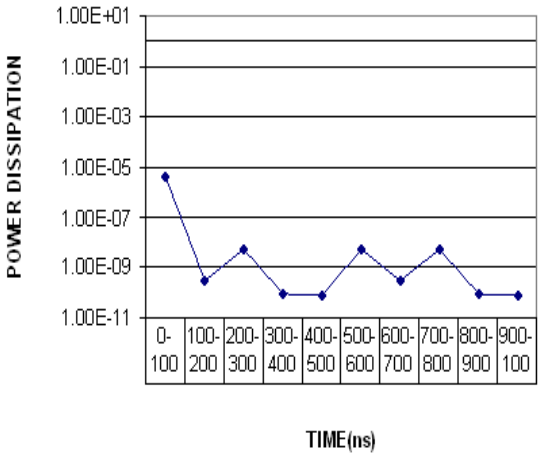


Figure 4: Power dissipation during stand by operation

During standby time, word line is off and both bit lines are pre-charged to $V_{CC.}$ In the first waveform, a leakage current cause voltage drop across word line of 0.95V maximum and minimum drop of 0.2V across the cell. The two output nodes showing stored values at the nodes are next shown in the fig. 4. Voltage at node vout2 stored is logic '1' i.e. 1.8V and voltage stored at the node vout1 is approaching logic '0' i.e. 0V. Middle waveform is showing the voltage at node vout2 at the last waveform is showing the voltage at the node vout1.

### 3.2 Write Operation

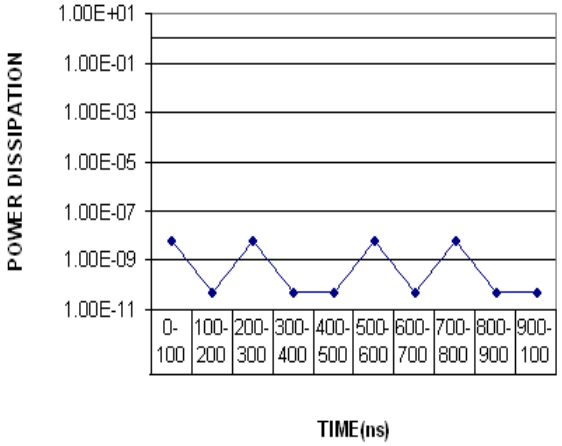


Figure 5: Power dissipation during write operation

It is correct to first write into the cell and then read the stored value. During the write operation, word line is set high and the voltage at the bit line BIT is not precharged and the bit line BIT_BAR is precharged to $V_{CC}$. The first waveform is showing the negative edge triggered pulse of 1.8V across the word line, fig. 5. The second waveform is showing the write logic '0' at the node vout2 and the last waveform is showing the write of logic '1' at the node vout1. Last two waveforms are showing spikes. In the write of logic '0', spikes are neglected. Also in the last waveform showing logic '1', the spikes range is very low i.e. 0.002V at the falling and rising edge of the word line. Hence, it is also negligible. The main use of negative edge triggered pulse is that it reduces delay and power dissipation in the cell in significant figures.

### 3.3 Read Operation

During the read operation, the word line is set high and both the bit lines are precharged to $V_{CC}$. The value written in the cell is confirmed in the read operation. The first waveform is showing the applied pulse to word line.

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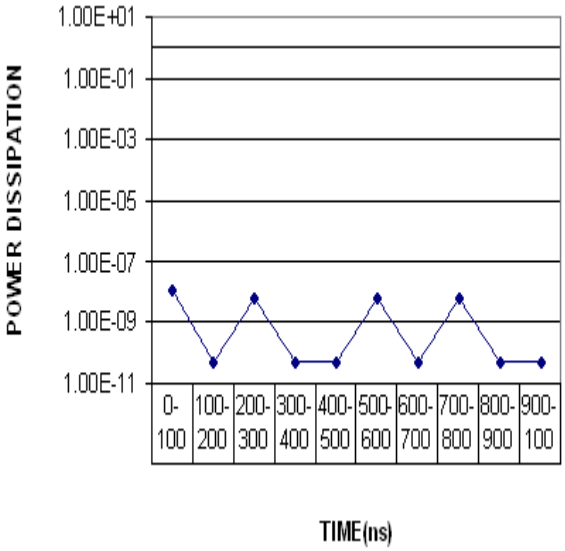


Figure 6: Power dissipation during right operation

The second pulse is showing the value stored is logic '0' across the node vout2 and the last waveform is showing the stored value at logic '1' across the node vout1. Again we can see the spike in the last waveform and its range is in between 2mV i.e. very low. But a significant power is saved and the speed of the cell is also increased.

### 4. Conclusion and Future Work

In the present paper, the power dissipation and delay in 6T SRAM has been reported. This work can also be elaborated to study various process parameters effect regarding width to length ratio and static noise margin in all the Cells that has been simulated. These factors are responsible for the stability of the Cell. Although the asymmetric technique is the latest in reducing the power dissipation in the cell configuration, yet some other techniques also exist. So, someone has to really study hard the publications and hands on experience on the simulation tool before working on new aspects. Now, the coming technology is nm CMOS technology and work has already started in this field. Memory is the most fundamental and integral part of all processors and programmable devices. So, we cannot say, we have achieved the best work in memory, it needs more and more exploration with the new design parameters and new system requirements.

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