ISSN (Online): 2230-7893
www.IJCEM.org

A Low Power 8-bit Magnitude Comparator with Small Transistor Count using Hybrid PTL/CMOS Logic

Geetanjali Sharma[1], Uma Nirmal[2], Yogesh Misra[3]
[1, 2, 3] Department of Electronics & Communication Engineering, Faculty of Engineering & Technology,
Mody Institute of Technology and Science (Deemed University)
Laxmangarh, Rajasthan-332311, India
[1]rhytham.1987@gmail.com, [2]nirmaluma1012@gmail.com, [3]yogeshmisra@yahoo.com

Abstract
Magnitude comparison is one of the basic functions used for sorting in microprocessor, digital signal processing, so a high performance, effective magnitude comparator is required. The main objective of this paper is to provide new low power, area solution for Very Large Scale Integration (VLSI) designers. At circuit level, Hybrid PTL/CMOS Logic style gives best results over CMOS only and PTL only. A fine cost-performance ratio comparator design based on modified 1's complement principle and conditional sum adder scheme using Hybrid PTL/CMOS logic style has been proposed in this paper and the proposed design has small power dissipation and less area over various supply voltages. Simulations based on BSIM 3V3 90nm CMOS technology. It shows an 8-b comparator of the proposed architecture only needs 154 transistors.

Keywords: magnitude comparator, modified *1's complement method, hybrid PTL/CMOS logic, power, area*

• 1. Introduction

In digital system the comparator is a very useful and basic arithmetic component. A compact, good cost benefit, high-performance ratio comparator plays an important role in almost all hardware sorters. One of the most important problems in computer science is sorting. Many fundamental processes in communication and computing systems require data sorting. Sorting network play a key role in the areas of parallel computing, multiprocessing and multi-access memories [1], [2].
As depicted in Fig. 1, compare and swap elements of data are vital for sorting. In conventional computer systems, instructions SUBTRACT and COMPARE often shares the hardware. This can reduce time complexity and cost. Fig. 2 displays an eight number three-level bitonic sorter. It uses 24 comparators to attain a higher performance target. To process long digit integer sorting the comparators array will become very large [2]. At this time, a high-performance and compact comparator core is very important.

Minimizing power dissipation for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Various parameters as power dissipation, speed, size, and wiring complexity of a logic circuit are affected by logic style used in that particular logic circuit [3]. Several Pass Transistor Logic (PTL) synthesis methods have been developed that have better performance, compared with traditional CMOS Logic for some arithmetic unit designs.
However PTL and CMOS have their respective advantages and disadvantages in terms of power dissipation, delay, and area, so at the circuit level, by mixing PTL with static CMOS that is hybrid PTL/CMOS one can achieve very low power dissipation, power delay product and area in the circuit. The power saving of hybrid PTL/CMOS logic circuits can reach up to more than 60 percent compared to conventional static CMOS circuit [3],[4].

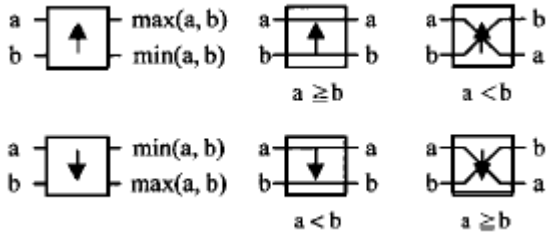

Fig. 1 Compare & swap elements are vital for sorting [5]

This paper deals with various types of 8 bit magnitude comparators using various logic styles and their comparative performance. A variety of magnitude comparators using static or dynamic logic styles have been reported in the literature [6]-[8]. Power dissipation and area used by these comparator circuits is relatively large.

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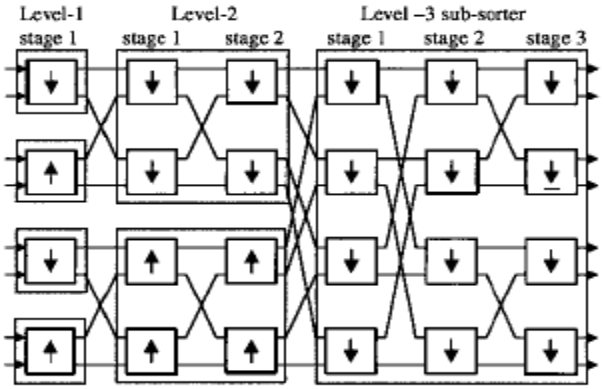


Fig. 2 A three-level bitonic sorter [5]

Comparison of various 8 bit magnitude comparators and their performances is done by using BSIM3V3 90nm technology. This paper proposed a fine cost-performance ratio comparator design based on conditional sum adder [9] scheme and modified 1's complement principle using hybrid PTL/CMOS logic style, the proposed design has low power dissipation transistor count.

• 2. Magnitude Comparator

2.1 Conventional Magnitude Comparator

A magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. An n bit magnitude comparator block is shown in Fig. 3 and it compares two n bit binary numbers A and B and produces three outputs: GT (A>B), EQ (A=B) and LT (A<B).

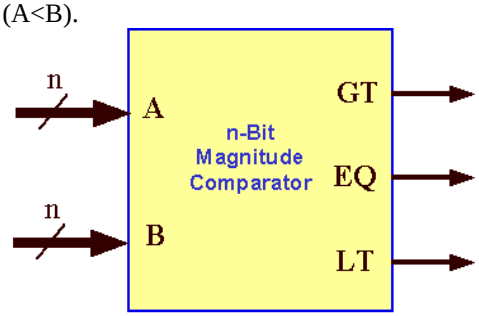


Fig. 3 A magnitude comparator block

Consider an example of a 4-bit magnitude comparator shown in Fig. 4 which compares two 4-bit words (A, B), each word having four Parallel Inputs (A0–A3, B0– B3); A3, B3 being the most significant inputs. Operation is not restricted to binary codes; the device will work with any monotonic code. Three outputs are provided: "A greater than B" (A>B), "A less than B" (A<B) and "A equal to B" (A=B).

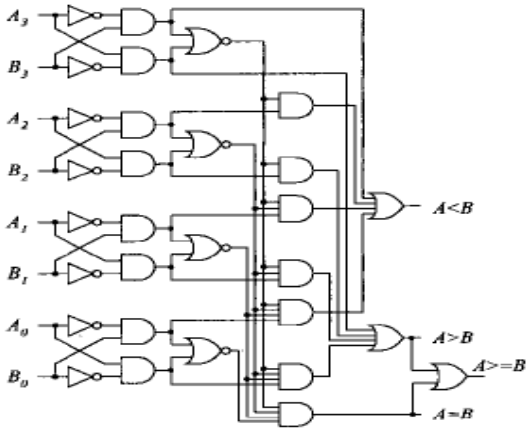
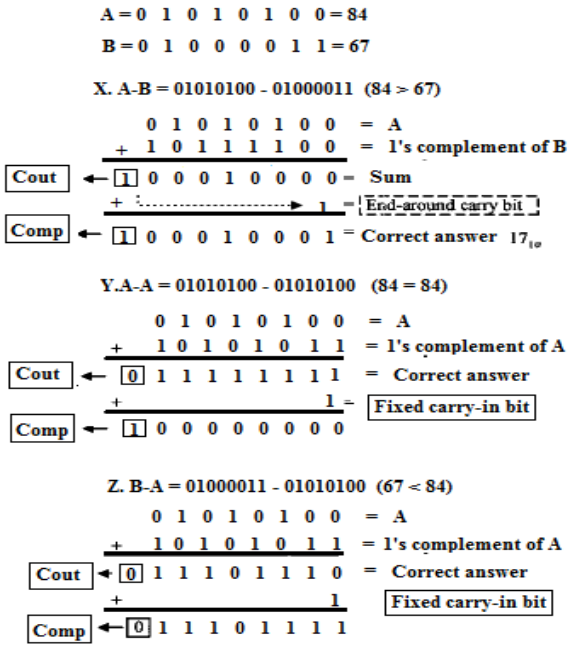


Fig. 4 Four bit magnitude comparator

In many applications, two outputs are enough: A≥B and A<B. In case of magnitude comparators 4-bit comparator is the basic constructive unit and cost complexity of a (2k)-bit comparator are often not only twice than a k-bit comparator, so implement a long bit-length comparator by the old scheme is uneconomical.

2.2 Improved Magnitude Comparator

Fig. 5 shows a modified 1's complement scheme. In this, if X >*Y*, bit Cout = 1 and if X ≤Y, bit Cout =0 so the only concerned is about carry out bit information.



Status bit	Cout	Comp
A > B	1	1
A = A	0	1
B < A	0	0

Fig. 5 Modified l's complement method for improved comparator design

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This method always adds a fixed carry after modification, so if X≥Y, bit Comp = 1 and if X<Y, bit Comp =O [5]. Thus the status of Comp bit gives output of comparison but using classic design in Fig. 4 two bits are needed to give the same information that is ineffective. In common discussions, both *two* numbers are positive but if two numbers are of different signs, then by directly comparing the sign bit answer can be obtained. If both two numbers are negative, the answer is just opposite. At this time the output signal Comp = Comp +Sign-bit and make the fixed carry-in bit = *0* always, and the condition is solved.

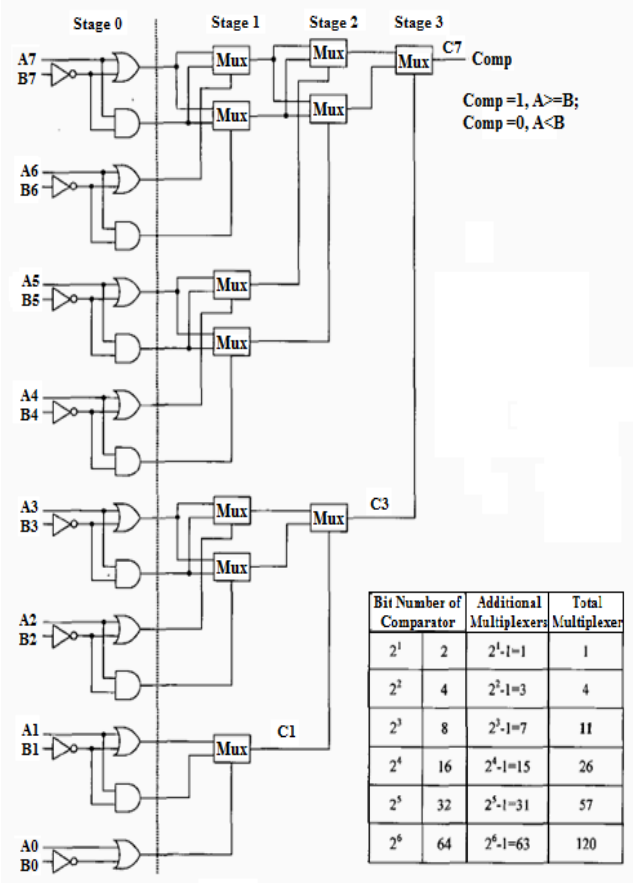

Fig. 6 An Eight bit improved magnitude comparator architecture using modified 1's complement and conditional sum adder design. [5]

This Conditional Sum Adder has been improved for high-performance applications [9]. Originally Carry = AB + AC + BC = AB + (A + B) C and if C=O than Carry =AB or if C=l than Carry = AB + (A+B) =A + B. The sum of MUX gates of N-bit comparator is,

$$\sum_{K=1}^{M}(2^{k}-1), \text{where } M = log_2 N$$

Consider an example of the improved 8 bit magnitude comparator architecture shown in Fig. 6 below. This 8-bit comparator needs 11(1+3+7) 2-to-1 multiplexers and eight inverters to generate complementary values of input B. The total gate count is eight inverters, eight two-input OR gates, seven two-input AND gates, and eleven 2-to-1 multiplexers [10].

From above scheme we can find the transistor count of the new design is less than that required in the conventional design.

3. CMOS Logic Style versus PTL Style

Pass-Transistor and CMOS Logic style have their respective advantages and disadvantages in terms of Power delay product, power dissipation, area and output driving capability [4]. Basically, CMOS fulfills all the requirements for ease-of-use of logic gates. On the other hand due to irregular transistor arrangements and high wiring requirements layout of pass-transistor cells is not as efficient and straightforward. Several Pass Transistor Logic (PTL) synthesis methods have been developed that have better performance, compared with traditional CMOS logic for some arithmetic unit designs [11]-[13] and are used to design large logic circuits [14]-[16]. A PTL synthesis method depends on PTL cell library that contains a wide variety of PTL logical cells constructed from few basic cells. Similarly a CMOS cell library usually contains tens or hundreds of logic cells, each with individual layouts.

4. Hybrid PTL/CMOS Logic Style

4.1 Need of Hybrid PTL/CMOS Logic Style

PTL has some advantages over static CMOS that it has the capability to implement a logic function with smaller number of transistor, smaller delay and less power dissipation [3], [4], [10], and [11]. For full swing output level-restoring logics may be required at the PTL output gates and these level-restoring logics will slow down the PTL circuits and increase the power dissipation as well.

Table I compares three basic logic circuits designed using CMOS and PTL using TSMC 90 nm technology. It shows that PTL based 4-to-1 multiplexer and XOR3 have smaller power (including dynamic power and static leakage power), power delay product and smaller area, but PTL is not universally better than CMOS for all types of logic structures, static CMOS can result in better implementations than PTL for NOR and NAND-intensive circuits[4].

Since CMOS and PTL have their respective advantages and disadvantages in terms of Power dissipation, power delay product and area, hybrid CMOS/PTL can give better results with respect to area, power and delay Therefore, mixed static CMOS/PTL synthesis is likely to be an attractive alternative in the future.

Hybrid PTL/CMOS logic style uses a hybrid combination of CMOS and Pass Transistor Logic style. This logic style contains advantages of both these logic styles. Binary

ISSN (Online): 2230-7893
www.IJCEM.org

decision diagrams (BDD) [4], [16] can be used to represents a logic function in Hybrid PTL/CMOS logic style.

4.2 Hybrid PTL/CMOS Logic Synthesis Flow

Hybrid PTL/CMOS logic synthesis embedded in the traditional standard cell-based design flow with Synopsys DC for the back-end placement and routing (P&R) and the front-end logic synthesis and Cadence SoC Encounter shown in Fig. 7 This design flow permit us to perform logic synthesis based on pure CMOS, pure PTL, or hybrid PTL/CMOS cell library, with various design constraints. So we may design PTL logic cells and basic cells, along with the corresponding synthesis flow for Hybrid PTL/CMOS synthesis as in fig. [12].

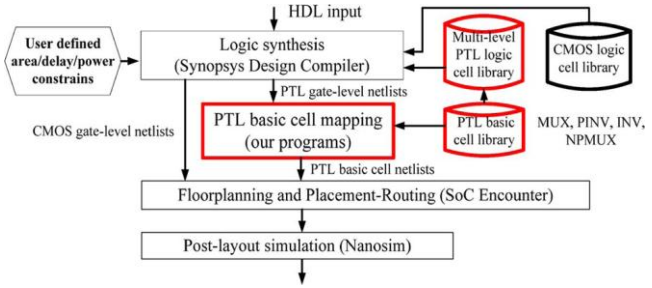

Fig. 7 Hybrid CMOS/PTL logic synthesis flow [17].

5. Comparison and Result

Implementation of 8 bit conventional magnitude comparator and improved magnitude comparator using CMOS, Pass transistor and Hybrid CMOS/PTL logic styles have been done at 90 nm BSIM3V3 technology. Power dissipation comparisons for 8 bit magnitude comparator using various logic styles over supply voltage (V_{dd}) range are shown in Fig. 8 and Fig. 9.Simulation results are shown in Table II.

Here Fig. 8 is depicting that CMOS based improved comparator shows less power dissipation than CMOS and Hybrid PTL/CMOS logic based conventional comparator over various V_{dd} and Fig. 9 depicted that hybrid PTL/CMOS based improved comparator shows less power dissipation than PTL and CMOS based improved comparator. Hybrid PTL/CMOS based improved comparator shows 10% to 60% less power dissipation than CMOS based conventional comparator and Hybrid PTL/CMOS based improved comparator shows 7% to 50% less power dissipation than Hybrid PTL/CMOS based conventional comparator. After comparison we can conclude that Hybrid PTL/CMOS based improved comparator has least power dissipation.

Fig. 10 shows area comparison of conventional 8 bit magnitude comparator using CMOS and Hybrid PTL/CMOS and improved magnitude comparator using CMOS, Pass Transistor, Hybrid PTL/CMOS Logic style. This shows that improved magnitude comparator using Hybrid PTL/CMOS logic style uses least number of transistors. It uses 65 % less area (no. of transistors) than CMOS Logic based conventional magnitude comparator.

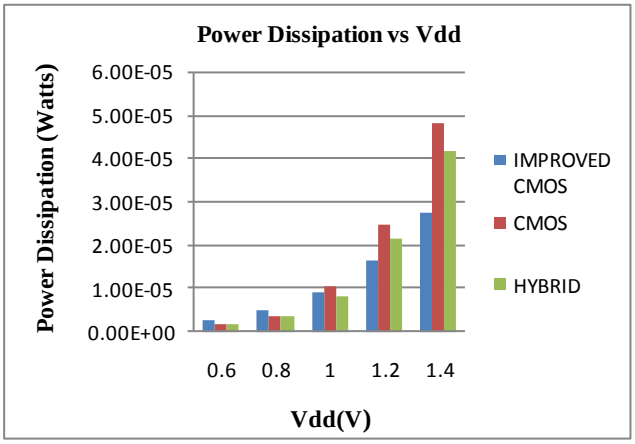

Fig. 8 Power dissipation comparison between conventional magnitude comparator using CMOS and Hybrid PTL/CMOS Logic style and improved magnitude comparator using CMOS Logic style versus V_{dd}.

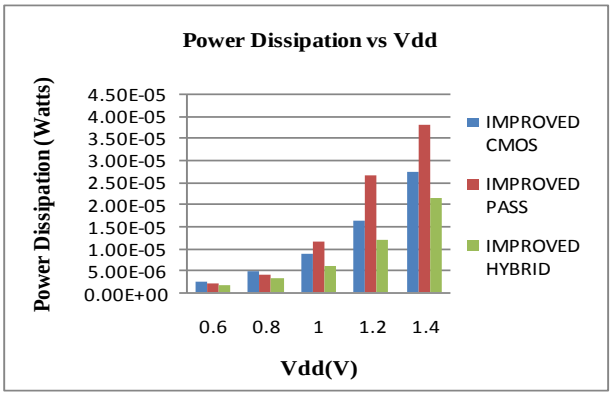

Fig. 9 Power dissipation comparison of improved magnitude comparator using CMOS, Pass Transisitor and Hybrid PTL/CMOS Logic style versus V_{dd}.

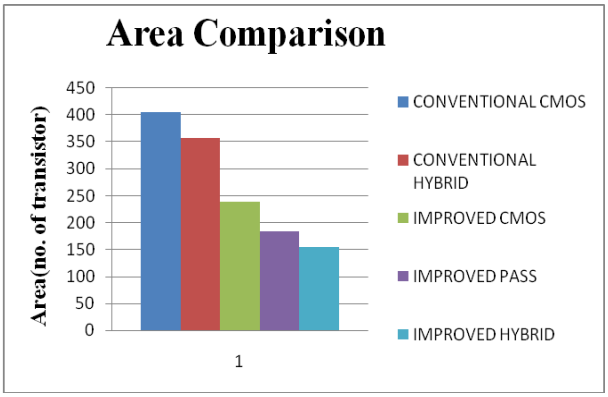

Fig. 10 Area comparison of 8 bit magnitude comparators using various Logic styles.

TABLE I: SIMULATION RESULTS OF BASIC CELLS OVER VARIOUS SUPPLY VOLTAGES [4]

Basic Logic Cells	Power Dissipation (µW)				Power - Delay Product (10^{-14})				Area (No. Of transistors)	
	V_{dd}=1.2V		V_{dd}=0.8V		V_{dd}=1.2V		V_{dd}=0.8V			
	CMOS	*PTL*	*CMOS*	*PTL*	*CMOS*	*PTL*	*CMOS*	*PTL*	*CMOS*	*PTL*
XOR	3.5	2.3	0.47	0.33	3.7	2.6	0.5	0.3	32	14
NOR	0.41	1.8	0.08	0.22	0.0082	0.039	0.0008	0.011	04	06
MUX	6.56	1.44	0.75	0.13	7.3	1.6	0.8	0.1	30	10

TABLE II: SIMULATION RESULTS OF 8 BIT MAGNITUDE COMPARATOR OVER VARIOUS SUPPLY VOLTAGES

Vdd(V)	Power Dissipation (µW)				
	CMOS	*Hybrid*	*Improved CMOS*	*Improved PTL*	*Improved Hybrid*
1.4	48.3	41.7	27.3	38.1	21.4
1.2	24.6	21.4	16.2	26.8	12
1	10.4	8.26	9.01	11.8	6.05
0.8	3.57	3.30	5.04	4.51	3.15
0.6	1.64	1.62	2.67	1.99	1.59

6. Conclusion

With power and area being a limiting factor in high density and high-performance VLSI designs, a great deal of effort has been made to explore low-power and area design options without sacrificing performance. Hybrid PTL/CMOS logic style used in this work provides us low power design as compared to CMOS and Pass Transistor Logic styles. It has been found that the transistor count, power dissipation of the improved comparator using Hybrid PTL/CMOS Logic style is less than that of the conventional comparator design. Proposed Improved comparator using Hybrid PTL/CMOS Logic style shows relatively large power savings over a range of supply voltage than other comparators. The comparisons of comparator design are based upon BSIM3V3 90nm technology in tanner EDA tool.

Acknowledgments

The authors wish to thank the Management, Dean-FET and the Head of Electronics & Communication Engineering of Mody Institute of Technology & Science (Deemed University), Laxmangarh (District Sikar), Rajasthan, India for providing all necessary support to carry out this research work successfully.

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Geetanjali Sharma was born in Rajasthan,India, in 1987. She received the B.Tech degree in Electronics and Communication Engineering from the University of Rajasthan, India in 2007. Since 2007 she is working as Assistant Professor in ECE department for Mody Institude of Technology and Science, Laxmangarh, Rajasthan(India). She is pusuing M.Tech in VLSI Design from MITS (Deemed) University, India. Her research interest includes VLSI design.

Uma Nirmal is working as Assistant Professor in ECE department for Mody Institude of Technology and Science, Laxmangarh, Rajasthan(India). She is pusuing M.Tech in VLSI Design from MITS (Deemed) University, India. Her research interest includes VLSI design.

Yogesh Misra having more than seventeen years of industrial and teaching experience is currently working as Assistant Professor in Mody Institute of Technology & Science (Deemed University), Laxmangarh. He also worked in U V Instruments (P) Ltd, a sugar mill automation company for many years. His research interest include VLSI CAD, VLSI embedded computing and soft computing. He also authored a book titled "Digital System Design using VHDL". He is life member of ISTE.