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FPGA Based Hardware Realization of DCT – II Independent Update Algorithm for Image Processing Applications

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Abstract

Discrete Cosine Transform (DCT) and Discrete Sine Transform (DST) are two transform compression techniques that are used extensively for data compression, most notably in audio, speech and image processing applications. Several algorithms for computation of DCT and DST coefficients have been developed so far, among which independent update algorithm seems to be the most promising technique for future applications. In this paper, the FPGA implementation of the DCT – II independent update algorithm has been undertaken and its performance is evaluated. Use of the above algorithm for applications like image intelligence, biometric systems, image duplication etc. is also discussed.

Keywords: *FPGA, DCT – II Independent Update Algorithm, Image Processing, Digital System Design, Hardware Software Co-simulation, Impulse C*

1. Introduction

Digital Signal Processing (DSP) involves the use of mathematics, algorithms and various physical techniques to manipulate signals after they have been converted to digital form. In most cases, these signals originate as sensory data from the real world. Once these signals are acquired, DSP can be used to analyze the signal from all possible domains such that some external need is satisfied that could either be control of some external system or enhanced sound quality or better image resolution, speech recognition, data compression etc.

When analogue signals representing information are acquired for processing, the size of the input data is very large (high bandwidth) and requires a lot of hardware to store and transmit it which increases the over-all cost of the device. For this reason, data is compressed to a suitable size which makes it convenient enough for storage and transmission by limited hardware resources designed within a limited budget. Various compression algorithms are present which can suitably reduce the size of a given data. However, transform compression is one method which has gained considerable favour in the recent years due to its multiple advantages like fast execution times, efficient algorithms, robust performance, high bandwidth reduction capability etc.

Discrete Cosine Transform (DCT) and Discrete Sine Transform (DST) are two transform compression algorithms that are used extensively for data compression, most notably in audio, speech and image processing applications. The DCT has been adopted as a standard for data compression in JPEG image and MPEG video file standards and with little modification in AAC, WMA and MP3 audio standards.

A lot of algorithmic research has been undertaken for the fast implementation of the DCT [1]. A large number of fast algorithms for computation of DCT coefficients can be found in the literature [2]. All these algorithms can be realized in hardware due to various properties of DCT such as orthogonality, preservation of information of a signal under transformation, separability etc. [3-4]. However, these fast algorithms can sometimes be computationally expensive for really large data sequences for example a very high resolution image. A computationally less expensive alternative is the update algorithm [5-8]. For the real-time processing of an infinite input sequence of data using update algorithm, a portion of the sequence is sampled and the transform is performed using definition. New data points are shifted in as and when they are available while the old data points are

shifted out. The transform of this new shifted sequence is then computed using the update algorithm.

In this paper an attempt has been made to realize the hardware implementation of update algorithm on a Field Programmable Gate Array. Although many update algorithms have been developed so far [6] [8] [9-10], they are not feasible for real-time applications as it requires simultaneous update of both DCT and DST coefficients. In [1], the independence of the DCT and DST coefficients was established and an update algorithm was developed feasible enough for fast real-time applications. Although the hardware implementation was also given for 1 and 4 point update, the implementation was however, more application specific (for compression needs). In case of compression, one simply needs to pass the DCT coefficients through a low pass filter to retain the low frequency coefficients containing maximum information. For this application, one can have a direct hardware mapping of the independent update algorithm without any significant performance overhead as it is faster than computing the DCT coefficients by definition anyway.

It was realized, however, that DCT of image can be used for other applications as well and hence a need was felt to develop the hardware in a manner that allows us to use it for multiple real-time applications. After careful analysis, it was discovered that one can speed up the execution of the update algorithm for fast and multiple real-time applications, if one introduces fine grain parallelism to this algorithm at the hardware level. In this paper, we have developed the hardware in accordance with this point of view. The hardware has been designed using Impulse C that allowed us to introduce this parallelism on a hardware level and have been synthesized in Xilinx's Virtex 6 FPGA.

2. DCT – II Independent Update Algorithm

The mathematical definition of type II DCT can be written as [11]:-

$$C_{II}(k) = \sqrt{\frac{2}{N}} P_k \sum_{x=0}^{N-1} f(x) \cos\left(\frac{(2x+1)k\pi}{2N}\right) \tag{1}$$

where the value of P_k = 1/sqrt(2) for k = 0 or N and 1 otherwise.

For k = 0, it can be seen that (1) reduces to

$$C_{II}(k=0) = \sqrt{\frac{1}{N}} \sum_{x=0}^{N-1} f(x) \tag{2}$$

This means that the first transform coefficient is the average value of the sample sequence of the input signal. This value is referred to as the DC coefficient while all other transform coefficients are referred to as AC coefficients.

In the presence of shifting data, (1) can be modified to include the sequence pointer n to keep track of points as [10]:-

$$C_{II}(n, k) = \sqrt{\frac{2}{N}} P_k \sum_{x=0}^{N-1} f(n-N+x) \cos\left(\frac{(2x+1)k\pi}{2N}\right) \tag{3}$$

From (3), the r-point independent update equation for DCT – II coefficients can be derived as [1]:-

$$\begin{aligned} C_{II}(n+r, k) &= 2\cos\left(\frac{rk\pi}{N}\right) C_{II}(n, k) - C_{II}(n-r, k) \\ &+ \sqrt{\frac{2}{N}} P_k \sin\frac{rk\pi}{N} \sum_{x=0}^{r-1} [f(n-N-x-1) - (-1)^k f(n-x-1)] \sin\frac{(2x+1)k\pi}{2N} \\ &+ \sqrt{\frac{2}{N}} P_k \sum_{x=0}^{r-1} [(-1)^k f(n+r-x-1) - f(n+r-N-x-1)] \cos\frac{(2x+1)k\pi}{2N} \\ &- \sqrt{\frac{2}{N}} P_k \cos\frac{rk\pi}{N} \sum_{x=0}^{r-1} [(-1)^k f(n-x-1) - f(n-N-x-1)] \cos\frac{(2x+1)k\pi}{2N} \end{aligned} \tag{4}$$

From this update equation, it is clear that to get the real-time updated coefficients of N point data taking r points at a time; we need DCT coefficients of the current and one previous time sequence. From these considerations, we can ascertain the flowchart of the update algorithm as shown in Fig. 1.

The flowchart roughly indicates the logic behind the update algorithm that can be utilized for its hardware implementation. The processing of the data starts by first determining if there is any previous data and the previous two time step DCT coefficients available as is required by the algorithm. If no such data and DCT coefficients exist then the system automatically calculates it by definition and stores it in memory. This process is repeated for the second sequence. The calculation of DCT by definition for the first two data sequences is called the pre-computation phase [1].

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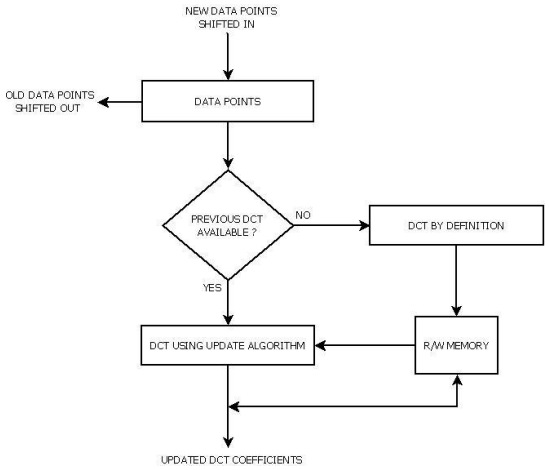

Fig. 1 Flowchart of the DCT – II Independent Update Algorithm

When the third data sequence arrives, the system enters in the update mode and utilizes the older DCT coefficients to calculate the new DCT coefficients. This process of calculating DCT coefficients by update algorithm continues as and when new data points are shifted in, which proves to be much faster than calculation of DCT coefficients by definition alone.

3. Hardware Implementation

The hardware implementation of the independent update algorithm for DCT – II has been done using Impulse C within the CoDeveloper 3.60 IDE and implemented in Xilinx's Virtex 6 FPGAs. Impulse C is a subset of standard ANSI C language which is specifically used for Hardware Software co-design. It is basically used for embedded and high performance computing applications. The greatest advantage in designing DSP hardware using Impulse C is the fine grain parallelism that it provides by virtue of system level pipelining and instruction scheduling which saves the number of clock cycles for computation and thus accelerates performance [12]. This feature provided by Impulse C allows us to accelerate the execution of the independent update algorithm and thus make it possible for use in multiple processing applications in real-time. Once the Impulse C code for the hardware is written, one can directly obtain the equivalent VHDL code optimized for the specific FPGA chosen which can be used for synthesis or use it within the CoDeveloper IDE for hardware software co-simulation.

The design works in 4 modes using mode select lines that actually indicate the resolution of the image on which the processing is performed. If "00" is given on the mode select lines, then the pixel values are represented with 8 bits. For "01", 9 bits word size is used. Similarly for "10", 10 bits word size and for "11" 12 bits word size is used. This has been done to ensure that the design can be used for a number of image processing tasks involving images of varying resolution. The design accepts parallel data input. A signal *next_in* indicates the start of the data word whenever it is high. Thereafter the data input rate is one bit per clock cycle until reaching the MSB. For a 1 point update process involving 8X8 image data, the device consumes 195 clock cycles (assuming 8 bit word size) which for a 100 MHz clock translates to 1.95 microseconds.

The following table shows the synthesis summary:-

Table 1: Synthesis Summary

Slice Logic Utilization	**Used**	**Available**	**% Utilization**
No. of slice registers	540	93,120	1%
No. of slice LUT	428	46,560	1%
No. of LUT – FF pair used	382	481	79%
No. of bonded IOBs	45	240	19%

The generated RTL schematic (using VHDL-only code) of the entire module is shown in Fig. 2 below while the RTL schematic of the hardware controller is shown in Fig. 3:-

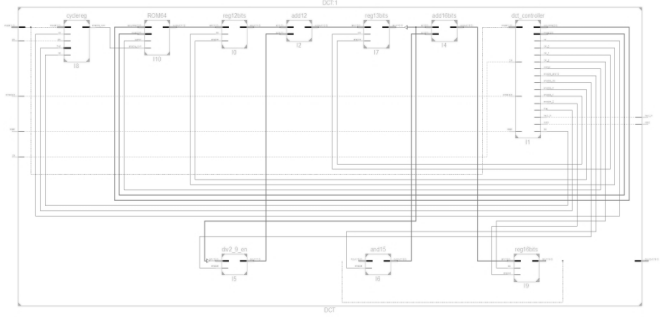

Fig. 2 Xilinx RTL Schematic of the DCT module

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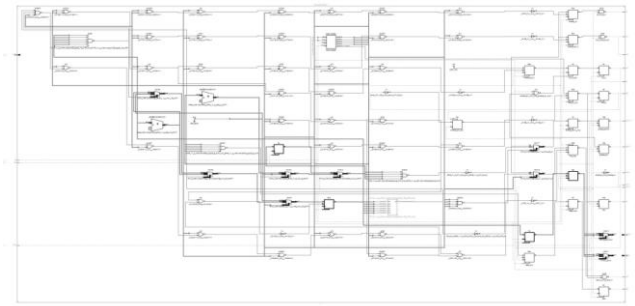

Fig. 3 Xilinx RTL Schematic of the DCT controller

4. Simulation Results

The designed hardware was tested and simulated for its accuracy. A grayscale image was chosen for simulation. Particular pixel values of the image were obtained using MATLAB Image Processing Toolbox which was then fed as input to the DCT hardware designed above.

The output is shown in Fig. 4 below. As can be clearly seen, the independent update algorithm does a reasonably good job in computing the DCT of an input data sequence.

Fig. 4 Test image and its corresponding DCT equivalent image

5. Performance Dependencies

Once fine grain parallelism was introduced in the independent update algorithm, the execution speed has dramatically increased. However, the performance of the hardware depends on certain crucial factors such as:-

1) The number of representation bits chosen for pixel values in the target image. This parameter is chosen by appropriate signals via mode select lines as said earlier. For 12 bits word size, time required for computation is 3.48 microseconds. Normally, the choice of representation bits will be dictated by the resolution demanded by the underlying application.

2) Number of cores on parallel FPGAs. It is possible to implement the design on multiple FPGAs and then operate them in parallel giving rise to super parallel architecture. Thus, computation on each FPGA will be as per fine grain parallelism (via the design created in this paper) while the parallel working of different FPGAs will be coarse grain parallelism. This can be done for multiple image DCT computation for image forensics and intelligence.

3) Area overhead. The implementation of the independent update algorithm with fine grain parallelism uses slightly more FPGA resources compared to the direct implementation. However, the authors believe that this can be suitably minimized by exploring different coding styles in Impulse C. The way an algorithm is expressed in code plays a major role in its execution time. Impulse C is capable enough to find interdependencies in the code and combine multiple statements into single instruction stages representing single clock cycle. However, this process can be manually controlled by the explicit use of compiler pragmas.

4) Power constraints. The performance of the hardware can also be judged from the power constraints of the final application in which the designed hardware will be used. The efficient hardware design of the independent update algorithm with fine grain parallelism with a view to minimize power consumption is currently under research by the authors.

6. Conclusion & Future Prospects

The FPGA implementation of the DCT – II independent update algorithm with fine grain parallelism has been successfully carried out which gives reasonably good results. The advantage of low power, low cost and reconfigurability offered by FPGAs allow us to implement the independent update algorithm for computationally complex image processing tasks in a much better manner than ASICs. The parallelization of the independent update algorithm speeds up the execution time considerably making it suitable for widespread image processing use in multiple applications.

Few applications where the FPGA based implementation of DCT – II independent update algorithm can be useful are as follows:-

a) Image authentication based biometric security systems as in [13] and [14].

b) Prevention of image duplication. Amidst the presence of such vast amount of visual rich media content, artists and photographers can copyright their images using DCT signature. A real image will have a unique DCT signature while a copy of that image from a different source will have a different DCT signature. Comparison between them can distinguish the real and the copied image.

c) Forensic image analysis. The DCT signature of the image can be used to gather specific image intelligence that can aid in crime investigation.

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